Dr. Sudhansu Mohan Biswal,Ph.D.

Name : SUDHANSU MOHAN BISWAL

Designation : Associate Professor

Department : Department of Electronics & Instrumentation Engineering

(JOINED THE INSTITUTE IN JAN 2007)

Contact : +91-9438788420,9861863662

Email : sudhansu.mohan@silicon.ac.in

RESEARCH INTERESTS

- ✓ Semiconductor devices modeling and simulation study
- ✓ VLSI Design
- ✓ IoT & Automation Control

Today the challenges CMOS technology is facing in terms of severe Short-channel effects (SCEs) arising from the extremely scaled dimensions has resulted in the need to explore new device architectures and design.The research interest of Dr Biswal spans around the study, discussion and investigation of the effect of diminishing MOS channel length on device characterizes and their remedies by novel unconventional device structures, highlighting his concept of MOSFET device physics and knowledge of scaling trends in MOSFET evolution using device modeling and TCAD simulation. The research of interest is to provide the impact of various device physics and device scaling on the RF performance analysis and investigation of various linearity matrices due to their dominant role for today's RF systems and circuits using analytical model and simulation

Academic Qualifications

Ph. D. (Engg) Maulana Abul Kalam Azad University of Technology, West Bengal, India

M. Tech. (Electronics & Communication Engg.), BPUT, Odisha

B. Tech. (AE&I), Utkal University, Odisha

Specialisation: Nano Electronics & Device engg.

Teaching Experience/Industrial Experience/Research Experience

Teaching Experience : More than 16 years

Research Experience : More than 7 years

PUBLICATIONS

JOURNAL

J1. **Biswal, S.M.**, Baral, B., De, D. and Sarkar, A., "Analytical subthreshold modeling of dual material gate engineered nano-scale junctionless surrounding gate MOSFET considering ECPE" ***Superlattices and Microstructures*, published by Elsevier** B.V., vol. *82*, pp.103-112*.,* 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140

J2. **Biswal, S.M.**, Baral, B., De, D. and Sarkar, A., "Study of effect of gate-length downscaling on the analog/RF performance and linearity investigation of InAs-based nanowire Tunnel FET" ***Superlattices and Microstructures***, **published by Elsevier** vol. 91, pp. 319-330, 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140

J3. **Biswal, S. M.***,* Baral, B.*, D.* De, and Sarkar A. "Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET "*Advances in Industrial Engineering and Management*, published by **American Scientific Publishers, USA,** vol. 5, no. 1, pp. 150-156, 2016, DOI: 10.7508/aiem. 2016.01.005.

J4. **Biswal, Sudhansu Mohan**, Biswajit Baral, Debashis De, and A. Sarkar. "Simulation and comparative study on analog/RF and linearity performance of III–V semiconductor-based staggered heterojunction and InAs nanowire (nw) Tunnel FET**."** ***Microsystem Technologies*** (2017) **SPRINGER:** 1-7 **Impact factor :1.513**

J5. Baral. B**., Biswal. S,** De. D*, and* Sarkar. A. "Effect of gate-length downscaling on the analog/RF and linearity performance of InAs-based nanowire tunnel FET ***"International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,* published by John Wiley & Sons Inc.,** vol. 30, no. 3-4, 2016, doi: 10.1002/jnm.2186,.(**SCI Indexed**) **Impact Factor: 0.833.**

J6. Baral, B.*,* **Biswal, S. M.***,* De, D.*, and* Sarkar A. " RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET" *Simulation: Transactions of the Society for Modeling and Simulation International*" published by **SAGE Publications, United Kingdom,** vol. 1-9, 2017 **(SCI Indexed) Impact Factor: 0.713**

J7. Baral, B.*,* **Biswal, S. M.***,* De, D.*, and* Sarkar A. "Effect of gate length downscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications & it's comparative study with conventional Mosfet"*Advances in Industrial Engineering and Management*, published by **American Scientific Publishers, USA** vol. 5, no. 1, 2016, pp. 130-137, DOI: 10.7508/aiem.2016.01.005.

J8. Swain, S., **Biswal, S. M.***,Das* S.,Adak S.,Baral B. " Performance Comparasion of InAs based DG-MOSFET with respect to SIO2 and Gate stack configuration"**Journal of Nanoscience & Nanotechnology-Asia,published by Betham Science.**Vol.9, 2019**(SCI Indexed) Impact factor : 0.78**

J9. Misra,S., **Biswal S.M.**,Baral B.,Swain S.,Sarkar A,Pati S. "Analytical modelling of Cyl-JLAMOSFET in subthreshold region using distinct device geometry"**Journal of Computaional Electronics:SPRINGER Publications,vol1-14, 2020(SCI Indexed) Impact factor:1.86 DOI:**10.1007/s10825-020-01560-z

CONFERENCE

C1. **Sudhansu Mohan Biswal**, Biswajit Baral, et al. "Study of effect of gate-length downscaling on the Analog/RF performance of Tunnel FET." International conference Nanocon 014*,* Pune, 14th &15th October 2014.

C2. **Sudhansu Mohan Biswal**, Biswajit Baral , et al. " Simulation and comparative study on Analog/rF performance of Silicon and InAs nanowire Tunnel FET " TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016), (MAKAUT).

C3. **Sudhansu Mohan Biswal**, Biswajit Baral, et al. " Analog/RFand Linearity Performance of staggered heterojunction Nanowire Tunnel FET for low power application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).

C4. **Sudhansu Mohan Biswal**, Biswajit Baral, et al. " Analog/RF performance and linearity investigation of Si-based double gate Tunnel FET " 1st International conference on Devices for Integrated Circuits(DevIC-2016).

C5. Biswajit Baral, **Sudhansu Mohan Biswal**, et al. " Performance Investigation of III-V Heterosturucture Underlap Double Gate MOSFET for System-On-Chip Application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).

C6. Biswajit Bara**l**, **Sudhansu Mohan Biswal**, et al. "Performance Analysis of Downscaled Triple Material Double Gate Junctionless MOSFET using High-K for Analog/mixed signal System-on-chip Applications." TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016). (MAKAUT)

C7. Biswajit Baral, **Sudhansu M Biswal**, et al. " Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th &15th October 2014.Payel Chand,

C8. Nikhil Agarwal, Biswajit Baral,**Sudhansu Mohan Biswal** " Comparative Study of Gate Underlap and Overlap in Junction-less DG-MOSFET with High k-Spacer through simulation" National conference on Recent Advances on electrical and electronics engg. (NCRAEEE-15),27th -28th March,2015, GIFT,Bhubaneswar.

C9. B.Baral, P.priya, R.Nayak, S. Pradhan, **S.M.Biswal** "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET"IEEE International Conference on Communication and Electronics System(ICCES-2017),19th-20th October 2017,Coimbatore.

C10. B.Baral, **S.M.Biswal,** P.Priya, S.K.Swain, S.Mishra "Impact of variation in barrier thickness on a Gate-Engineered TM-DG Heterostructure MOSFET to suppress SCEs and Analog, RF, Linearity performance investigation for SOC applications" IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.

C11. S.K.Swain, S. Adak, **S.M.Biswal**, B.Baral, S.Parija "Comparision of Linearity Performance of InP Based DG MOSFETs with Gate Stack SIO2 and HfO2" IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.

C12. **S.M.Biswal**, B.Baral, S.K.Swain, S.K.Pati "Performance Analysis of Down Scaling Effect of Si Based SRG Tunnel FET." IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.

C13. S.Mishra, **S.M.Biswal**, B.Baral, S.K.Swain, S.K.Pati "Study of Effect of Down Scaling on the Analog/RF Performance of Gate All Around JL MOSFET." IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.

C14. B.Baral, P.priya, R.Nayak, S. Pradhan,**S.M.Biswal** "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET"IEEE International Conference on Communication and Electronics System(ICCES-2017),19th-20th October 2017, Coimbatore

C15. Swain, Sanjit Kumar, Sarosij Adak, **Sudhansu Mohan Biswal**, Biswajit Baral, and Saradiya Parija. "Comparison of Linearity Performance of InAs Based

DG-MOSFETs with Gate Stack, SiO2 and HfO2." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 242-246. IEEE, 2018.

C16. Das, Satish Kumar, **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, and Biswajit Baral. "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET." In International Conference on Intelligent Computing and Communication Technologies, pp. 803-812. Springer, Singapore, 2019.

C17. **Biswal, Sudhansu Mohan**, Biswajit Baral, Sanjit Kumar Swain, and Sudhansu Kumar Pati. "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 344-348. IEEE, 2018.

C18. **Biswal, Sudhansu Mohan**, Sanjit Kumar Swain, Biswajit Baral, Debasish Nayak, Umakanta Nanda, Satish Kumar Das &Dhananja Tripthy."Performance Analysis of Staggered Heterojunction based SRG TFET biosensor for health IoT application." In 2019 Devices for Integrated Circuit (DevIC), pp. 493-496. IEEE, 2019.

C19. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, **Sudhansu Mohan Biswal,** Dhananjaya Tripthy, Sanjit Kumar Swain, Biswajit Baral, and Satish Kumar Das. "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination." In 2019 Devices for Integrated Circuit (DevIC), pp. 314-317. IEEE, 2019.

C20. Tripathy, Dhananjaya, Debasish Nayak, **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, Biswajit Baral, and Satish Kumar Das. "A Low Power LNA using Current Reused Technique for UWB Application." In 2019 Devices for Integrated Circuit (DevIC), pp. 310-313. IEEE, 2019.

C21. Baral, Biswajit, **Sudhansu Mohan Biswal**, Sanjit Swain, Satish Kumar Das, Debasish Nayak, and Dhananjaya Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC pplications." In 2019 Devices for Integrated Circuit (DevIC), pp. 505-509. IEEE, 2019.

C22. Das, Satish K., Sanjit K. Swain,**Sudhansu M. Biswal,**Debasish Nayak,Umakanta Nanda, Biswajit Baral, and Dhananjaya Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET."In 2019 Devices for Integrated Circuit (DevIC), pp.365-369. IEEE, 2019.

BOOK CHAPTER

- **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, Jyoti Ranjan Sahoo, Anupam K. Swain, Kunal Routaray, Umakanta Nanda, Birendra Biswal, "A Comparative Study Of Junctionless Triple-Material Cylindrical Surrounding Gate Tunnel Fet", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 793-801, 03 November 2018.
- Umakanta Nanda, Debasish Nayak, Sushant Kumar Pattnaik, Sanjit Kumar Swain, **Sudhansu Mohan Biswal**, Birendra Biswal, "Design And Performance Analysis Of Current Starved Voltage Controlled Oscillator", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 235-246, 03 November 2018.
- Sanjit Kumar Swain, **Sudhansu Mohan Biswal**, Umakanta Nanda, D. Siva Patro, Suraj Kumar Nayak, Birendra Biswal, "Impact Of P-Gan Gate Length On Performance Of Algan/Gan Normally-Off Hemt Devices", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 803-809, 03 November 2018.

ANY OTHER

NATIONAL & INTERNATIONAL SEMINAR/WORKSHOP/ CONFERENCE/ FDP PARTICIPATED, PRESENTED & ORGANIZED:

1) Seminar on "A refresher course on *VLSI technologies*" at Sakthi Mariamman Engineering College, Chennai on 3rd September 2005.
2) Workshop on "Creative thinking and collaborative learning" at sSilicon Institute of Technology, Bhubaneswar on 10th -14th December 2007
3) National workshop on Advanced Signal & Image processing (WASIP-2008) at Silicon Institute of Technology, Bhubaneswar on 11-13th Dec 2008.
4) FDP programme on *MATLAB and Its Applications,* Organized by BPUT, jointly with NITTTR Kolkata on 12-16th October 2009.
5) National workshop on "Advanced Signal Processing and Communication" *(WASPC-2010)* at Silicon Institute of Technology, Bhubaneswar on 8th to 10th January 2010.
6) National workshop on "Advanced Signal Processing application in Electronics & Telecommunication" (WASET-2010) at GMRIT, Andhra Pradesh on 19th & 20th February 2010.
7) National seminar on "Recent trends in contemporary communications" (RTCC-2010) held at Silicon Institute of Technology, Bhubaneswar from 3rd to 4th march 2010.
8) National workshop on "Image and Signal Processing"(WISP-2011) at Silicon Institute of Technology, Bhubaneswar on 29-30thJan 2011.
9) National conference in "Future trends in information and communication technology & application" held at Silicon Institute of Technology, Bhubaneswar from 10th to 11th September 2011.
10) Seminar on "Professional Ethics & Human Values for Engineers" Held at Silicon Institute of Technology, Bhubaneswar In collaboration with power Grid Corporation of India from 23rd-24th Dec 2011.
11) A Hand's on training experience in LAB VIEW by National Instruments at Silicon Institute of Technology, Bhubaneswar from 14th to 16th February 2012.
12) National workshop on Next generation wireless communication and networking (WNWCN-2012) at Silicon Institute of Technology, Bhubaneswar on 24th to 25th February 2012.
13) National workshop on "Swarm Intelligence: Theory and Applications "held at IIT Bhubaneswar on 25th-27th May 2012.
14) International conference on communication, circuits and systems (ic^{3}s-2012) held at KIIT University, BBSR from 5th -7th October 2012.
15) FDP on 'Shikshak' at Silicon Institute of Technology, Bhubaneswar on 28th-29th December 2012
16) 1st Industry–academia workshop on VLSI held at BVB college of Engineering and technology, Hubli on 11th to 12th January 2013.
17) National workshop on "VLSI Signal Processing: Efficient Design and Implementation" at Silicon Institute of Technology, Bhubaneswar on 15th-18th March, 2013.
18) NMEICT(MHRD) sponsored Two week ISTE workshop on"Analog Electronics" conducted by IIT Kharagpur at Silicon Institute of Technology, BBSR on 4th -14th june, 2013.
19) AICTE sponsored National Conference on "Next Generation Wireless communication & Networking"SNWCN-2013 at KIST,BBSR on 23rd -24th August 2013.
20) AICTE sponsored National Seminar on "Speech Signal Processing & its Application"SSPA-13 at BCET, Balasore on 20th -21st Sept. 2013.
21) AICTE sponsored National workshop on "VLSI signal processing: Efficient Design and Implementation" (VLSISP-2013) at Silicon institute of Technology, Bhubaneswar on 14th-16th Nov,2013.

22) Professional training on Virtual Instrumentation using LabVIEW at Silicon Institute of Technology on 28thNov.to 4th Dec, 2013.
23) NMEICT (MHRD) sponsored FDP programme on "Signal & Systems" conducted by IIT Kharagpur held at Silicon Institute of Technology, Bhubaneswar from 2nd -12th January, 2014.
24) IEEE (EDS) Kolkata chapter Sponsored National workshop on "Advanced Nano Device & its Application"(NWANDA-2014) at Silicon Institute of Technology, BBSR on 17th-18th January, 2014.
25) National seminar on "Signal & Image Processing"(NSSIP-2014) held at Silicon Institute of Technology, Bhubaneswar on 20th Sept,2014.
26) Presented Paper at 3rd International Conference NANOCON 014 held at Bharati Vidyapeetha University,Pune on 14th -15th Oct,2014.
27) IEEE(EDS)Bhubaneswar Kolkata chapter Sponsored Mini-Colloquium on "Advanced Electron Devices & Circuits" at KIIT University, Bhubaneswar on 3rd -4th December, 2014.
28) NMEICT (MHRD) sponsored 2 week ISTE workshop on "Control Systems" conducted by IIT Kharagpur held at Silicon Institute of Technology, Bhubaneswar from 2nd -12th December, 2014.
29) Presented paper at International Conference on Information Technology (ICIT-2014) held at Silicon Institute of Technology, Bhubaneswar from 23rd - 24th December,2014.
30) Presented paper at International Conference on Information Technology (ICIT-2014) held at Silicon Institute of Technology, Bhubaneswar from 23rd - 24th December, 2014.
31) National workshop on "Signal & image processing"(NWSIP-2015) at Silicon Institute of Technology, Bhubaneswar on 9th -10th Oct, 2015.
32) NMEICT (MHRD) sponsored 2 week ISTE STTP on "Technical Communication" conducted by IIT Bombay held at Silicon Institute of Technology, Bhubaneswar from 8th Oct. to 5th Dec., 2015.
33) Presented Paper at National Conference on "Recent Advances on Electrical & Electronics Engineering" (NCRAEEE-2015) held at GIFT, Bhubaneswar on 27th-28th March 2015.
34) Presented Paper at National Conference on "Recent Advances on Electrical & Electronics Engineering"(NCRAEEE-2015) held at GIFT, Bhubaneswar on 27th-28th March 2015.
35) National workshop on "Recent Trends in Mobile Communication" (RTMC-2016) at Silicon Institute of Technology, Bhubaneswar on 22nd -23rd Jan, 2016.
36) IEEE(EDS)Bhubaneswar Kolkata chapter Sponsored Mini-Colloquium on "Advanced CMOS based Nano Devices" (MCACND-2016) at Silicon Institute of Technology, Bhubaneswar on 3rd-4th Dec,2016
37) Presented paper at 1st International Conference on "Devices for Integrated Circuits" (DevIc-2016) held at Kalyani Govt. Engg. College Kolkata from 29th -30th March,2016.
38) National workshop on "Industrial Automation & Control"(NWIAC-2016) at Silicon Institute of Technology, Bhubaneswar on 18th -19th March, 2016
39) Presented paper at TEQIP-II, WBUT Sponsored "1st International Conference on Nanocomputing and Nanobiotechnology" (NanoBiocon-2016) held at MAKAUT, West Bengal on 3rd -5th Oct.2016.
40) Presented paper at 2nd International Conference on "Devices for Integrated Circuits"(DevIc-2017) held at ,Kalyani Govt. Engg. College Kolkata from 23rd -24th March,2017.
41) NMEICT(MHRD) sponsored 2 week ISTE STTP on "CMOS,Mixed Signal & Radio Frequency VLSI Design" conducted by IIT Kharagpur held at Silicon Institute of Technology, Bhubaneswar from 30th Jan. to 4th Feb.,2017.

42) AICTE sponsored FDP on "Design of Micro-Optical Components using Advanced software Tools" held at GITA, Bhubaneswar from 27th Nov. to 9th Dec. 2017.
43) IEEE(EDS)Kolkata chapter Sponsored National workshop on "Recent Trends in VLSI Devices & Circuits"(RTVDC-2018) at Silicon Institute of Technology, Bhubaneswar on 23rd -24th march,2018.
44) TEQIP-III sponsored Workshop on IoT and Sensor Embedded Applications(ISEA-2019) at Silicon Institute of Technology, Bhubaneswar on 16th -20th Dec 2019
45) TEQIP-III sponsored Workshop on Nanotechnology and Embedded Systems(NES-2019) at Silicon Institute of Technology, Bhubaneswar on 27th -30th Dec 2019
46) TEQIP-III sponsored Short Term Training Program on Industrial Automation and Control for Industry 4.0 at Silicon Institute of Technology, Bhubaneswar on 25th-29th Oct 2019
47) Faculty Development program on Electronics System Design Manufacturing using OrCAD simulation Tools, By Entuple Technology at Silicon Institute of Technology, Bhubaneswar on 8th -10th Aug 2019
48) National Workshop on Advanced Communications and Signal Processing(NWACSP-2019) at Silicon Institute of Technology, Bhubaneswar on 27th-29th Sept 2019.
49) Summer course on VLSI Design And EDA Tools at Silicon Institute of Technology, Bhubaneswar on 1st -17th May 2006.
50) FDP on IOT for Emerging technical Application In Smart City at Trident Academy of Technolog, Bhubaneswar on 3rd-15th Dec. 2019
51) Participated in TEDxSITB "Half Empty Half Filled" at Silicon Institute of Technology, Bhubaneswar on 15th Dec 2019.
52) TEQIP-III sponsored 3 days Workshop on Functional Materials for Emerging Technology (FMET-2020) at Silicon Institute of Technology, Bhubaneswar on 13th -15th FEB 2020.
53) TEQIP-III sponsored 5 days Workshop on Machine Learning for Data Science using Python(MLDSP-2020) at Silicon Institute of Technology, Bhubaneswar on 15th -19th January 2020.
54) Presented paper in 3rd International conference on Devices for Integrated Circuits(DevIC-2019) at KGEC,Kolkata on 23rd-24th March 2019.
55) AICTE Recognised Online FDP on Low power VLSI Design By ECE department of NITTR Chandigarh on 20th -24th April 2020.
56) Participated online FDP on Nanotechnology by Saveetha Engg. college , Chennai from 29th -3rd July 2020.
57) Participated One week webinar series on "Wireless Communication towards 5G" by Singhad Institute of Technology and Science, Pune on 25-29th May 2020.
58) Attended 2 days online workshop on ML & AI Using Covid-19 Virus Data Analysis By FINLAND Labs, In asso. With National Social Summit, IIT Roorkee on 16th -17th May 2020
59) Participated online FDP on Recent Advancement in Signal processing ML and next generation wireless Acess Network RASWAN-2020, by IGIT Saranga on 11th-24th june
60) Presented paper in International conference IEEE EDKCON 2018 at The PRIDE Hotel, KOLKATA on 24th -25th Nov.2018.

SOFTWARE SKILLS

- Silvaco
- MATLAB
- Labview
- Pspise
- PLC/SCADA