



Dr. Debasish Nayak, Ph.D.

Name : Debasish Nayak

Designation : Sr. Asst. Professor

Department : Department of Electronics and Instrumentation
(JOINED THE INSTITUTE IN 2009)

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RESEARCH INTERESTS

- ✓ Static Random Access Memory design and performance enhancement
- ✓ Study of digital circuit and performance enhancement
- ✓ Mixed signal and VLSI design
- ✓ SRAM design for IoT node
- ✓ Device level modification intended for SRAM design

Academic Qualifications

Post-Doctorate: University of Texas, Edinburg, USA

Ph. D: (VLSI) National institute of Technology, Rourkela, Odisha, India

M. Tech: (Electronics & Telecommunication Engg.), BPUT, Odisha, India

B.Tech: (Electrical & Electronics Engg.), BPUT, Odisha, India

Specialization: VLSI.

Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching experience-7 years
- ✓ Industry experience- 1Year 3 months (SASKEN comm. Tech.)
- ✓ Research experience- 5 years (Post-Doctoral Research at University of Texas & Research Scholar in National Institute of Technology, Rourkela)

JOURNAL:

- [1]. **D. Nayak**, D.P. Acharya, K. Mahapatra, "An improved energy efficient SRAM cell for access over a wide frequency range", **Solid-State Electronics (Elsevier)**, vol. 126, pp. 14-22, Dec 2016. **(SCI Impact Factor 1.492)**.
- [2]. **D. Nayak**, D.P. Acharya, K. Mahapatra, "Current Starving the SRAM Cell: A Strategy to Improve Cell Stability and Power", **Circuit, System and Signal Processing (Springer)**, vol. 36, Issue 8, pp. 3047-3070, Aug 2017. **(SCI Impact Factor 1.922)**.
- [3]. **D. Nayak**, D.P. Acharya, K. Mahapatra, "A Read Disturbance Free Differential Read SRAM Cell for Low Power and Reliable Cache in Embedded Processor", **AEU - International Journal of Electronics and Communications (Elsevier)**, vol. 74, pp. 192-197, April 2017. **(SCI Impact Factor 2.853)**.
- [4]. **D. Nayak**, D.P. Acharya, P.K. Rout, U. Nanda, "A high stable 8T-SRAM with bit interleaving capability for minimization of soft error rate", **Microelectronics Journal (Elsevier)**, vol. 73, pp. 43-51, March 2018. **(SCI Impact Factor 1.284)**.
- [5]. U. Nanda, D.P. Acharya, **D. Nayak**, P.K. Rout, "High performance PLL for multiband GSM applications", **International Journal of Nanoparticles (Inderscience)**, vol. 10, no. 3, pp. 244-258, **(Scopus, SCImago Journal Rank 0.121)**
- [6]. **D. Nayak**, D.P. Acharya, P. K. Rout, U. Nanda, "A Novel Charge Recycle Read Write Assist Technique for Energy Efficient and Fast 20nm 8T-SRAM Array", **Solid-State Electronics (Elsevier)**, vol. 148, pp. 43-50, Oct 2018. **(SCI Impact Factor 1.492)**
- [7]. **D. Nayak**, P. K. Rout, S. Sahu, D.P. Acharya, U. Nanda, D. Tripathy, "A Indirect Read based SRAM was designed to reduce power and improve speed and stability", **Microelectronics Journal (Elsevier)**, vol. 97, pp. 01-11, Mar 2020. **(SCI Impact Factor 1.284)**
- [8]. U. Nanda, D.P. Acharya, **D. Nayak**, "Process Variation Tolerant Wide-band Fast PLL with Reduced Phase Noise using Adaptive Duty Cycle Control Strategy", **International Journal of Electronics(Taylor & Francis)**, (Accepted author version posted online: 07 Jul 2020), **(SCI Impact Factor 1.004)**
- [9]. U. Nanda, **D. Nayak**, "Low voltage high performance high swing cascode current mirror", **American Journal of Circuits, Systems and Signal Processing, Public Science Framework**, American Institute of Science, Vol. 1, no. 2, pages 28–31, 2015.

CONFERENCE:

- [1]. P.K. Rout, **D. Nayak**, D.P. Acharya, "A novel low power 3T inverter", in Proc. of **IEEE International conference on Advanced Electronic Systems (ICAES)**, Sept. 2013, pp. 221-224, Pilani, India

- [2]. **D. Nayak**, D.P. Acharya, P. K. Rout, K. Mahapatra, "Design of low-leakage and high writable proposed SRAM cell structure", in Proc. of **IEEE International conference on Electronics and Communication System (ICECS)**, Feb. 2014, pp. 1-5, Coimbatore, India
- [3]. P.K. Rout, D.P. Acharya, G. panda, **D. Nayak**, "Process Corner Variation Aware Design of Low Power Current Starved VCO", in Proc. of **IEEE International conference on Electronics and Communication System (ICECS)**, Feb. 2014, pp. 6-10, Coimbatore, India
- [4]. **D. Nayak**, D.P. Acharya, K. Mahapatra, "Power efficient design of a novel SRAM cell with higher write ability", in Proc. of **IEEE India Conference (INDICON)**, Dec. 2015, pp. 1-6 (2015), Delhi, India
- [5]. S. N. Panda, S. Padhi, V. Phanindra, U. Nanda, S. K. Pattnaik and **D. Nayak**, "Design and implementation of SRAM macro unit", in Proc. of **IEEE International Conference on Trends in Electronics and Informatics (ICEI)**, May. 2017, pp. 119-123 (2017), Tirunelvely, India
- [6]. S. K. Pattnaik, U. Nanda, **D. Nayak**, S. R. Mohapatra, A. B. Nayak and A. Mallick, "Design and implementation of different types of full adders in ALU and leakage minimization", in Proc. of **IEEE International Conference on Trends in Electronics and Informatics (ICEI)**, May. 2017, pp. 924-927 (2017), Tirunelvely, India
- [7]. **D. Nayak**, U. Nanda, P. K. Rout, S. M. Biswal, D. Tripathy, S. K. Swain, B. Baral, S. K. Das, "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination", in Proc. of **IEEE International Conference on Devices for Integrated Circuit (DevIC)**, March. 2019, pp. 314-317 (2019), Kalyani, India.
- [8]. D. Tripathy, **D. Nayak**, S. M. Biswal, S. K. Swain, B. Baral, S. K. Das, "A Low Power LNA using Current Reused Technique for UWB Application", in Proc. of **IEEE International Conference on Devices for Integrated Circuit (DevIC)**, March. 2019, pp. 310-313 (2019), Kalyani, India
- [9]. N. K. Mucheli, U. Nanda, **D. Nayak**, P. K. Rout, S. K. Swain, S. K. Das, S. M. Biswal, "Smart Power Theft Detection System", in Proc. of **IEEE International Conference on Devices for Integrated Circuit (DevIC)**, March. 2019, pp. 302-305 (2019), Kalyani, India
- [10]. S. M. Biswal, S. K. Swain, B. Baral, **D. Nayak**, U. Nanda, S. K. Das, D. Tripathy, "Performance Analysis of Staggered Heterojunction based SRG TFET biosensor for health IoT application", in Proc. of **IEEE International Conference on Devices for Integrated Circuit (DevIC)**, March. 2019, pp. 493-496 (2019), Kalyani, India
- [11]. S. K. Swain, S. K. Das, S. M. Biswal, S. Adak, U. Nanda, A. A. Sahoo, **D. Nayak**, D. Tripathy, "Effect of High-K Spacer on the Performance of Non-Uniformly doped DG-MOSFET", in Proc. of **IEEE International Conference on Devices for Integrated Circuit (DevIC)**, March. 2019, pp. 510-514 (2019), Kalyani, India
- [12]. S. K. Das, S. K. Swain, S. M. Biswal, **D. Nayak**, U. Nanda, B. Baral, D. Tripathy, "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET", in Proc. of **IEEE International Conference on Devices**

for *Integrated Circuit (DevIC)*, March. 2019, pp. 365-369 (2019), Kalyani, India

- [13]. B. Baral, S. M. Biswal, S. K. Swain, **D. Nayak**, S. K. Das, D. Tripathy, "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications", in *Proc. of IEEE International Conference on Devices for Integrated Circuit (DevIC)*, March. 2019, pp. 505-509 (2019), Kalyani, India
- [14].

BOOK CHAPTER:

- [1]. U. Nanda, **D. Nayak**, S. K. Pattnaik, S. K. Swain, S. M. Biswal and B. Biswal, "Design and Performance Analysis of Current Starved Voltage Controlled Oscillator" in *Microelectronics, Electromagnetics and Telecommunications*, (**Springer**), pp. 235-246,
- [2]. **D. Nayak**, D. P. Achary, P. K. Rout, U. Nanda, "Design and analysis of variability aware FinFET-based SRAM circuit design" in *VLSI and Post-CMOS Electronics, Vol. 2: Devices, circuits and interconnects*, (**IET**), Chapter 6, pp.101-122.
- [3]. U. Nanda, D. P. Achary, P. K. Rout, **D. Nayak**, B. Jena, "Performance Linked Phase Locked Loop Architectures: Recent Developments", in *Advanced VLSI Design and Testability Issues*, 1st Edition, (**CRC Press**), **Taylor and Francis**, Chapter 16, pp. 271-290.

ANY OTHER

Projects undergoing
/ applied

PROJECTS:

- [1]. Design and fabrication of a low power area optimized SRAM array in XFAB technology for IoT application (**Chip fabricated**)