Mr. Santunu Sarangi

Name :Mr. Santunu Sarangi

Designation : Asst. Professor

Department : Electronics and Instrumentation Engineering

(JOINED THE INSTITUTE IN JANUARY, 2019)

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RESEARCH INTERESTS

Analog and Mixed Signal VLSI Design:

- ✓ High Speed SerDes (Serializer-Deserializer) Design
- ✓ Equalizer and its adaptation mechanism design for SerDes Systems.
- ✓ Voltage Controlled Oscillator (VCO) and Phase Locked Loop (PLL) Design
- ✓ Current Mode Logic (CML) based High-speed component Design
- ✓ Low noise and Low-tempco bandgap reference (BGR) Design
- ✓ Custom Analog and RF layout design and it's optimization
- ✓ Post fabrication measurement and characterization

ACADEMIC QALIFICATION

Ph. D. (High Frequency VLSI Design) Cont. from IIT Kharagpur, India

M. Tech. (Semiconductor Device Modeling) NIT Rourkela, India

Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience: 2 Years
- ✓ Industry Experience: 3+ years
- ✓ Research Experience: 6+ years
- ✓ Consultancy Experience: 1+ Years

PUBLICATIONS

JOURNAL& CONFERENCES

[1]. **Santunu Sarangi**, Dhananjaya Tripathy, Subhra Sutapa Mahapatra and Saroj Rout, "A Power- and Area-Efficient CMOS Bandgap Reference Circuit with an Integrated Voltage-Reference Branch" MoSICom 2020: Modelling, Simulation and Intelligent Computing pp 144-154, Jan, 2020

[2]. Indranil Som, **Santunu Sarangi** and T. K. Bhattacharyya, "A 7.1-GHz 0.7-mW programmable counter with fast EOC generation in 65-nm CMOS", IEEE Trans. Circuits Syst. II Exp. Briefs, Jan. 2020

[3]. Indranil Som, **Santunu Sarangi** and T K Bhattacharyya, " Development of a Low Jitter Multi Gigabit SerDes System" Poster Presentation, IESAVISION Global Summit, February 19-20, 2019, Bangaluru, India.

[4]. **Santunu Sarangi**, Shiv Bhushan, Abirmoya Santra, Sarvesh Dubey, Satyabrata Jit, Pramod Kumar Tiwari, "A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs", Superlattices and Microstructures, Vol. 60, 2013, pp. 263-279.

[5]. Shiv Bhushan, **Santunu Sarangi**, Gopi Krishna Saramekala; Abirmoy Santra, Sarvesh Dubey, Pramod Kumar Tiwari "An Analytical Model for The Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETS with a Strained-Silicon (S-Si) Channel On Silicon-Germanium (SiGe) Substrates", Journal of Semiconductor Technology and Science, Volume 13, Issue 4, 2013, Pp.367-380.

[6]. Shiv Bhushan, **Santunu Sarangi**, Abirmoya Santra, Mirgender Kumar, Sarvesh Dubey, S. Jit and P. K. Tiwari, "An Analytical Surface Potential Model for Strained-Si On Silicon germanium MOSFET Including the Effects of Interface Charges" Journal of Electron Devices, Vol. 15, 2012, pp. 1285-1290.

[7]. **S. Sarangi**, A. Santra, S. Bhushan, K. S. Gopi, S. Dubey and P. K. Tiwari, "An Analytical Surface Potential Modeling of Fully-Depleted Symmetrical Double-Gate (DG) Strained-Si MOSFETs Including the Effect of Interface Charges," *2013 Students Conference on Engineering and Systems (SCES)*, Allahabad, 2013, pp. 1-5.

[8]. **S. Sarangi**, S. Bhushan, S. G. Krishna, A. Santra and P. K. Tiwari, "A simulation-based study of gate misalignment effects in triple-material double-gate (TMDG) MOSFETs," *2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s)*, Kottayam, 2013, pp. 486-489.

PATENTS

[1]. **Santunu Sarangi**, Indranil Som, and T. K. Bhattacharyya, "On-chip jitter measurement circuit for high speed data and clock", **Indian Patent filed, Filing No: 201931004744, Feb 2019.**

[2]. Indranil Som, **Santunu Sarangi**, and T. K. Bhattacharyya, "High-speed voltage controlled CML hysteresis delay cell and ring oscillator using the same", **Indian Patent filed, Filing No: 201931004949, Feb 2019**

ANY OTHER

Book Chapter
Conferences attended

[1]. Working as an ***Analog and Mixed Signal IP design consultant*** in Sevya Multimedia Technologies Pvt. Ltd.

[2]. Worked as a Teaching Assistant in ISTE STTP on CMOS, Mixed Signal and Radio Frequency VLSI Design Organized by IIT Kharagpur on 2016 (This workshop was held under the National Mission on Education through ICT (MHRD), India).

[3]. Attended as a Technical Export in CMOS and RF VLSI short-term course organised by NIT Sikkim on 2016 and 2017.

[4]. Worked as a track chair in VLSI track of IEEE TechSym 2016 conference, organized by IIT Kharagpur student branch.