Prakash Kumar Rout, Ph.D.

Designation : Additional Professor

Department : Department of Electronics & Communication Engg.

(JOINED THE INSTITUTE IN 17TH JUNE 2002)

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RESEARCH INTERESTS:

VLSI Design & Semiconductor Devices (Analysis and Design):

- ✓ Analog and Mixed Signal VLSI Design
- ✓ Digital VLSI Design
- ✓ Design, Simulation and Study of Semiconductor Devices like MOSFET, DGMOSFET, Tunnel FET, FinFETetc.

Academic Qualifications:

Ph.D. (Electronics and Communication Engineering, Specialization: Analog VLSI Design), NIT Rourkela

M.Tech. (Electronics and Telecommunication Engineering, Specialization: Communication Systems Engineering), KIIT University, Bhubaneswar

Teaching Experience/Industrial Experience/Research Experience:

Teaching Experience: 19+ Years

- ✓ Silicon Institute of Technology, Bhubaneswar: June 2002 to Till Date.

Research Experience: 12 Years

PUBLICATIONS

JOURNAL& CONFERENCES:

[1]. P.K.Rout, D.P. Acharya and G. Panda "A Multiobjective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO" IEEE Transaction on Semiconductor Manufacturing, Vol-27, Issue-1, Pages: 43-50, Feb. 2014. DOI.10.1109/TSM.2013.2295423

[2]. P.K.Rout, D.P. Acharya and G. Panda "Fast Physical Design of CMOS ROs for Optimal Performance using Constrained NSGA-II" AEU - International Journal of Electronics and Communications, Elsevier, Vol-69 (2015), Pages: 1233–1242, May 2015. http://dx.doi.org/10.1016/j.aeue.2015.05.004

[3]. D.Nayak, D.P. Acharya, P.K.Rout, and U.K.Nanda "A high stable 8T-SRAM with bit interleaving capability for minimization of soft error rate" Microelectronics Journal (Elsevier), Vol-73, Pages: 43-51, Jan. 2018.https://doi.org/10.1016/j.mejo.2018.01.008

[4]. D.Nayak, D.P. Acharya, P.K.Rout, and U.K.Nanda, "A novel charge recycle read write assist technique for energy efficient and fast 20 nm 8T-SRAM array" Solid State Electronics(Elsevier), Vol-148, Pages: 43-50, Oct. 2018.https://doi.org/10.1016/j.sse.2018.07.005

[5]. P.K.Rout, D.P. Acharya and G. Panda,"Design of a Novel Current Starved VCO via Constrained Geometric Programming" International Journal of Computer Applications (IJCA)-2011, Vol-3,Pages:37-40.ISSN: 0975 - 8887.NY, USA.

[6]. P.K.Rout, B.P.Panda,D.P. Acharya and G. Panda,"Analysis and Design of a 1GHz PLL for Fast Phase and Frequency Acquisition" International Journal of Signal and Imaging Systems Engineering (IJSISE)-2011 Publisher – Inderscience. 2014 Vol. 7 No. 1 Pages:30-37(Geneva,Swizerland) ISSN online: 1748-0701 :ISSN print: 1748-0698 .

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[8]. J Sarangi,Umakanta Nanda, P.K. Rout,"Study of Recent Charge Pump Circuits in Phase Locked Loop", I.J. Modern Education and Computer Science, Aug 2016, 8, 59-65 ISSN: 2075-0161.
DOI: 10.5815/ijmecs.2016.08.08

[9]. P.K.Rout, D.P. Acharya and G. Panda,"Digital Circuit Placement in FPGA based on Efficient Particle Swarm Optimization Techniques" 5thInternational Conference on Industrial and Information Systems-2010(ICIIS-2010), NIT, Surathkal. Page(s):224 – 227, Date: 29-07-2010 to 01-08-2010. Print ISBN:978-1-4244-6651-1.

[10]. P.K.Rout, D.P. Acharya and G. Panda,"Novel PSO based FPGA Placement Techniques" International Conference on Computer and Communication Technology (ICCCT-2010), MNNIT,Allahabad. Pages:630-634, Date 17-19 Sept. 2010, ISBN: 978-1-4244-9034-9

[11]. P.K.Rout, B.P.Panda,D.P. Acharya and G. Panda,"Analysis and Design of a 1GHz PLL for Fast Phase and Frequency Acquisition" International Conference on Electronic Systems-2011(ICES-2011), NIT, Rourkela. Date:7-9 Jan. 2011.

[12]. P.K.Rout and D.P. Acharya "Design of CMOS Ring Oscillator Using CMODE" International Conference on Energy, Automation and Signal (ICEAS-2011), SOA University, Bhubaneswar. Pages: 412-417, Date:28 - 30 Dec 2011.ISBN: 978-1-4673-0136-7. **Electronic ISBN:**978-1-4673-0136-7, **Print ISBN:**978-1-4673-0137-4.

[13]. P.K.Rout, D.P. Acharya and G. Panda,"Design of LC VCO for optimal figure of merit performance using CMODE" International Conference on Recent Advances in Information Technology (RAIT-2012), Dhanbad, India.Pages: 761 – 764, Date:15-17 March 2012, ISBN:978-1-4577-0694-3.

[14]. P.K.Rout, D.P. Acharya and G. Panda,"Design of Low Power 3.3-4 GHz LC VCO using CMODE " National Conference on Emerging Trends and Applications in Computer Science (NCETACS-2012), St. Anthony's College Shillong, Meghalaya. Pages: 717 – 720, Date: 25-26 March 2013, Print ISBN:978-1-4673-5037-2.

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[16]. P.K.Rout, D.P. Acharya and G. Panda,"Constrained Multi objective Optimization based Design of CMOS Ring Oscillator" International Conference on Computer Communication and Informatics (ICCCI 2014), Sri Shakthi Institute of Engineering and Technology, Coimbatore.Pages:1-5, Date: 3-5 Jan. 2014, ISBN: 978-1-4799-2353-3.

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[18]. D. Nayak,D.P. Acharya, P.K. Rout and K.K. Mahapatra, "Design of Low-Leakage and High Writable Proposed SRAM cell Structure" International Conference on Electronics and Communication System (ICECS-14), Karpagam College of Engineering, Coimbatore. Pages: 1-5, Date: 13-14 Feb. 2014, ISBN: 978-1-4799-2321-2.

[19]. NK Mucheli, U Nanda, D Nayak, PK Rout, SK Swain, SK Das, SM Biswal, "Smart Power Theft Detection System" 2019 Devices for Integrated Circuit (DevIC), 302-305. Kalyani Government Engineering College, West Bengal.23-24 March, 2019, Kalyani, Nadia, India(3rd Conference),ISBN: 978-1-5386-6722-4,

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[21]. Utpal Das, Shuvabrata Bandopadhaya, Prakash Kumar Rout, "Quality of Service Analysis of Massive MIMO Wireless System with Time Division Duplexing" 2018 International Conference on Applied Electromagnetics, Signal Processing and Communication (AESPC),pages:1-4, Vol-1,22-24, Oct. 2018.KIIT School of Electronics Engineering, Bhubaneswar. **Electronic ISBN:**978-1-5386-8333-0, **ISBN:**978-1-5386-8334-7, **DOI:** 10.1109/AESPC44649.2018.9033282

[22]. D Nayak, U Nanda, PK Rout, SM Biswal, D Tripathy, SK Swain, B Baral, "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination" 2019 Devices for Integrated Circuit (DevIC), 314-317.

[23]. D Nayak, PK Rout, S Sahu, DP Acharya, U Nanda, D Tripathy "A novel indirect read technique based SRAM with ability to charge recycle and differential read for low power consumption, high stability and performance" Microelectronics Journal Vol-97, Issue-6, Pages:1-11, 104723, 2020.https://doi.org/10.1016/j.mejo.2020.104723

[24]. U Nanda, DP Acharya, D Nayak, PK Rout"Modelling and Optimization of Phase Locked Loop under Constrained Channel Length and Width of MOSFETs" Silicon, Vol-13, Issue-1, Pages:1-7, 2021. https://doi.org/10.1007/s12633-021-00967-y

[25]. PK Rout, DP Acharya, D Nayak, U Nanda "Design of robust analog integrated circuit based on process corner performance variability minimization" Integration : The VLSI Journal, Volume 94, 2024, 102100. https://doi.org/10.1016/j.vlsi.2023.102100

ANY OTHER

Book Chapter

Book Chapters:

[1]. **Prakash Kumar Rout**, Debiprasad Priyabrata Acharya and Umakanta Nanda, "Advances in Analog Integrated Circuit Optimization: A Survey" Chapter-15, ''Handbook of Research on Applied Optimization Methodologies in Manufacturing Systems'', IGI Global, USA, Nov. 2017, ISBN13: 9781522529446.

[2]. Debasish Nayak, Debiprasad Priyabrata Acharya, **Prakash Kumar Rout** and Umakanta Nanda "Design and analysis of variability aware FinFET-based SRAM circuit design" Page:101-122,Chapter -6: Book Name: VLSI and Post-CMOS Electronics,Volume 2: Devices, circuits and interconnects, IET Publication,ISBN 978-1-83953-053-1 (Volume 2 hardback).(Sept. 2019)

[3]. Umakanta Nanda, Debiprasad Priyabrata Acharya, **Prakash Kumar Rout**, Debasish Nayak, and Biswajit Jena" Performance Linked Phase Locked Loop Architectures: Recent Developments"Book Chapter: published in CRC Press (Taylor & Francis.).Pages: 271-290(Chapter-16)(Book Name: Advanced VLSI Design and Testability Issues), ISBN: 978-0-367- 49282-3(19th August 2020)

Conferences attended

Conferences attended:

[1]. P.K.Rout, D.P. Acharya and G. Panda, "Constrained Multi objective Optimization based Design of CMOS Ring Oscillator" International Conference on Computer Communication and Informatics (ICCCI 2014), Sri Shakthi Institute of Engineering and Technology, Coimbatore.Pages:1-5, Date: 3-5 Jan. 2014, ISBN: 978-1-4799-2353-3.