



Biswajit Baral, Ph.D.

Designation : Associate Professor
Department : Department of Electronics & Communication Engg.
(JOINED THE INSTITUTE IN 2006)
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RESEARCH INTERESTS

- ✓ Semiconductor devices modeling and simulation study
- ✓ VLSI Design

Academic Qualifications

- Ph. D. (Electronics & Communication) in MAKAUT, West Bengal, India
- M. Tech. (Electronics & Communication Engg.), BPUT, Odisha
- B. Tech. (ETC), BPUT, Odisha

Teaching Experience/Industrial Experience/Research Experience

- Teaching Experience : More than 16 years
- Research Experience : More than 12 years

PUBLICATIONS:

JOURNAL & CONFERENCES

Journals:

1. **Baral, B.**, Das, A. K., De, D., and Sarkar, A. "An analytical model of triple-material double-gatemetaloxide-semiconductorfield-effect transistor to suppress short-channeffects" *International Journal of NumericalModelling: Electronic Networks, Devices and Fields*, published by John Wiley& Sons Inc.,vol. 29, no.1, pp. 47-62,2015,doi:10.1002/jnm.2044. (**SCI INDEXED**) Impact Factor: 0.622
2. **Baral, B.**, Biswal, S.,De, D., and Sarkar, A. "Effect of gate-lengthdownscaling on the analog/RF and linearity performance of InAs-basednanowire tunnel FET" *International Journal of NumericalModelling: Electronic Networks, Devices and Fields*, published by John Wiley& Sons Inc., vol. 30, no. 3-4, 2016, doi: 10.1002/jnm. 2186,. (**SCI INDEXED**) Impact Factor: 0.622
3. **Baral, B.**, Biswal, S. M., De, D., and Sarkar A. " ARF/Analog and Linearity performance of a Junctionless Double Gate MOSFET" *Simulation: Transactions of the Society for Modeling and Simulation International*" published by SAGE Publications, United Kingdom, vol. 1-9, 2017 (**SCI INDEXED**) Impact Factor: 0.713
4. **Baral, B.**, Biswal, S. M., De, D., and Sarkar A. "Effect of gatelengthdownscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications &it's comparative studywithconventionalMosfet" *Advances in Industrial Engineering and Management*, published by American ScientificPublishers, USA vol. 5, no. 1, 2016, pp. 130-137, DOI: 10.7508/aiem.2016.01.005.
5. Biswal, S.M., **Baral, B.**, De, D. and Sarkar, A., "Analytical subthreshold modeling of dual materialgateengineerednano-scalejunctionlessurroundinggate MOSFET considering ECPE" *Superlattices and Microstructures*, published by Elsevier B.V., vol. 82, pp.103-112., 2016 (**SCI INDEXED**) Impact Factor: 2.123, 5-Year Impact Factor: 2.140
6. Biswal, S.M., **Baral, B.**, De, D. and Sarkar, A., "Study of effect of gate-lengthdownscaling on the analog/RF performance and linearity investigation of InAs-basednanowire Tunnel FET" *Superlattices and Microstructures*, vol. 91,

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- pp. 319-330, 2016 (**SCI Indexed**) Impact Factor: 2.123, 5-Year Impact Factor: 2.140
7. Biswal, S. M., **Baral, B.**, D. De, and Sarkar A. "Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET" *Advances in Industrial Engineering and Management*, published by American Scientific Publishers, USA, vol. 5, no. 1, pp. 150-156, 2016, DOI: 10.7508/aiem.2016.01.005.
 8. Biswal, Sudhansu Mohan, **Biswajit Baral**, Debashis De, and A. Sarkar. "Simulation and comparative study on analog/RF and linearity performance of III-V semi-conductor-based staggered heterojunction and InAs nanowire (nw) Tunnel FET." *Microsystem Technologies* (2017): 1-7.
 9. Sanjit Kumar Swain*, Sudhansu Mohan Biswal, Satish Kumar Das, Sarosij Adak and **Biswajit Baral**, "Performance Comparison of InAs Based DG-MOSFET with Respect to SiO₂ and Gate Stack Configuration", *Nanoscience & Nanotechnology-Asia* (2019) 9:1. <https://doi.org/10.2174/2210681209666190919094434>

Conferences:

1. **Biswajit Baral**, Sudhansu Mohan Biswal, et al. "Performance Investigation of III-V Heterostructure Underlap Double Gate MOSFET for System-On-Chip Application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).
2. **Biswajit Baral**, Sudhansu Mohan Biswal, et al. "Performance Analysis of Downscaled Triple Material Double Gate Junctionless MOSFET using High-K for Analog/mixed signal System-on-chip Applications." TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016). (MAKAUT)
3. **Biswajit Baral**, Jagruti Padhee, et al. "Effect of gate length downscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications & its comparative study with conventional Mosfet" 1st International conference on Devices for Integrated Circuits (DevIC-2016).
4. **Biswajit Baral**, Sudhansu M Biswal, et al. "Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th & 15th October 2014.
5. Sudhansu M Biswal, **Biswajit Baral**, et al. "Study of effect of gate length downscaling on the Analog/RF performance of Tunnel FET." International conference Nanocon 014, Pune, 14th & 15th October 2014.
6. Sudhansu Mohan Biswal, **Biswajit Baral**, et al. "Simulation and comparative study on Analog/rF performance of Silicon and InAs nanowire Tunnel FET " TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016), (MAKAUT).
7. Sudhansu Mohan Biswal, **Biswajit Baral**, et al. "Analog/RF and Linearity Performance of staggered heterojunction Nanowire Tunnel FET for low power application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).
8. Sudhansu Mohan Biswal, **Biswajit Baral**, et al. "Analog/RF performance and linearity investigation of Si-based double gate Tunnel FET " 1st International conference on Devices for Integrated Circuits (DevIC-2016).
9. Prateek Singh, Sahed Akhtar, **Biswajit Baral**, "A Comparison study of RF and Analog Performance of a JL-DG MOSFET with different types of Channel material through simulation" 1st International conference ICIT-2014, 23rd-24th Dec 2014, SIT Bhubaneswar.
10. Payel Chand, Nikhil Agarwal, **Biswajit Baral**, "Comparative Study of Gate Underlap and Overlap in Junction-less DG-MOSFET with High k-Spacer through simulation" National conference on Recent Advances on electrical and electronics engg. (NCRAEEE-15), 27th -28th March, 2015, GIFT, Bhubaneswar.
11. R. Pattnaik, **B. Baral** et al. "Comparative performance analysis of JL DG-MOSFET with Underlap JL DG-MOSFET " National conference on Recent Advances on

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- electrical and electronics engg. (NCRAEEE-15), 27th -28th March, 2015, GIFT, Bhubaneswar
12. R.K.Majhi, S.Das, S.K.Kar, **B.Baral** "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications " 1st International conference ICIT-2014, 23rd -24th Dec 2014, SIT Bhubaneswar.
 13. **B.Baral**, P.priya, R.Nayak, S. Pradhan, S.M.Biswal "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET" IEEE International Conference on Communication and Electronics System (ICCES-2017), 19th-20th October 2017, Coimbatore
 14. Swain, Sanjit Kumar, Sarosij Adak, Sudhansu Mohan Biswal, **Biswajit Baral**, and Saradiya Parija. "Comparison of Linearity Performance of InAs Based DG-MOSFETs with Gate Stack, SiO₂ and HfO₂." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 242-246. IEEE, 2018.
 15. Das, Satish Kumar, Sudhansu Mohan Biswal, Sanjit Kumar Swain, and **Biswajit Baral**. "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET." In International Conference on Intelligent Computing and Communication Technologies, pp. 803-812. Springer, Singapore, 2019.
 16. Biswal, Sudhansu Mohan, **Biswajit Baral**, Sanjit Kumar Swain, and Sudhansu Kumar Pati. "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 344-348. IEEE, 2018.
 17. Biswal, Sudhansu Mohan, Sanjit Kumar Swain, **Biswajit Baral**, Debasish Nayak, Umakanta Nanda, Satish Kumar Das & Dhananjaya Tripathy. "Performance Analysis of Staggered Heterojunction based SRG TFET biosensor for health IoT application." In 2019 Devices for Integrated Circuit (DevIC), pp. 493-496. IEEE, 2019.
 18. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, Sudhansu Mohan Biswal, Dhananjaya Tripathy, Sanjit Kumar Swain, **Biswajit Baral**, and Satish Kumar Das. "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination." In 2019 Devices for Integrated Circuit (DevIC), pp. 314-317. IEEE, 2019.
 19. Tripathy, Dhananjaya, Debasish Nayak, Sudhansu Mohan Biswal, Sanjit Kumar Swain, **Biswajit Baral**, and Satish Kumar Das. "A Low Power LNA using Current Reused Technique for UWB Application." In 2019 Devices for Integrated Circuit (DevIC), pp. 310-313. IEEE, 2019.
 20. **Baral**, **Biswajit**, Sudhansu Mohan Biswal, Sanjit Swain, Satish Kumar Das, Debasish Nayak, and Dhananjaya Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications." In 2019 Devices for Integrated Circuit (DevIC), pp. 505-509. IEEE, 2019.
 21. Das, Satish K., Sanjit K. Swain, Sudhansu M. Biswal, Debasish Nayak, Umakanta Nanda, **Biswajit Baral**, and Dhananjaya Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET." In 2019 Devices for Integrated Circuit (DevIC), pp. 365-369. IEEE, 2019.

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