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Designation: Assistant Professor

Department: Department of Electronics and Communication Engineering

(JOINED THE INSTITUTE IN JULY, 2018)

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RESEARCH INTERESTS

- Semiconductor Device Modeling
- Bandgap Engineered Devices
- Reliability analysis of advanced heterostructure Devices

Academic Qualifications

Ph. D. (Electronics), Siksha „O“ Anusandhan (Deemed to be University), India

M. Tech. (VLSI & Embedded System Design), BPUT, Odisha, India

Teaching Experience/Industrial Experience/Research Experience

Teaching Experience: 4 years

Research Experience: 8 years

PUBLICATIONS

JOURNAL & CONFERENCES

JOURNALS:

1. **Sanghamitra Das**, Tara Prasanna Dash, Devika Jena, Eelena Mohapatra and Chinmay Kumar Maiti, "Strain-engineering in AlGaIn/GaN HEMTs: impact of silicon nitride passivation layer on electrical performance," *Physica Scripta*, Vol. 96, 124074.
2. **Sanghamitra Das**, Tara Prasanna Dash, Suprava Dey, Chinmay Kumar Maiti, NBTI Studies in GaAs p-MOSFETs, *Test Engineering and Management*, Vol. 82, pp. 2384 – 2390, 2020
3. **Sanghamitra Das**, S. Dey, T. P. Dash, E. Mohapatra, J. Jena and C. K. Maiti, "Impact of NBTI and Hot Carrier Stress on nanowire Characteristics," *Nanomaterials and Energy*, vol. 8, pp.1-7, 2019.
4. **Sanghamitra Das**, T. P. Dash, S. Dey, R. K. Nanda and C. K. Maiti, "Reliability Studies on Biaxially Tensile Strained-Si Channel p-MOSFETs," *International Journal of Microstructure and Materials Properties*, vol.14, pp. 28-46, 2019.
5. **Sanghamitra Das**, T. P. Dash and C. K. Maiti, "Negative Bias Temperature Instability in Strained-Si MOSFETs,"

- International Journal of Nano and Bio Materials (IJNBM), vol. 7, pp. 299 – 310, 2018.
6. **Sanghamitra Das**, T. P. Dash and C. K. Maiti, "Effects of Hot-Carrier Degradation on the Low-Frequency Noise in Strained-Si p-MOSFETs," International Journal of Nanoparticle (IJNP), vol.10, pp. 58-76, 2018.
 7. D. Pradhan, **Sanghamitra Das** and T. P. Dash, "Study of strained-Si p-channel MOSFETs with HfO₂ gatedielectric," Superlattices and Microstructures, vol. 98, pp. 203-207, 2016.
 8. T. P. Dash, **Sanghamitra Das**, S. Dey, and C. K. Maiti, "Electro-Thermal Assessment of Heterojunction Tunnel-FET for Low-Power Digital Circuits," International Journal of Nanoparticle, vol. 11, pp. 154-162, 2019.
 9. T. P. Dash, S. Dey, **Sanghamitra Das**, J. Jena, E. Mohapatra, and C. K. Maiti, "Performance Comparison of Strained-SiGe and Bulk-Si Channel FinFETs at 7N Technology Node," Journal of Micromechanics and Microengineering, vol. 29, pp. 104001, 2019.
 10. T. P. Dash, Suprava Dey, **Sanghamitra Das**, Eleena Mohapatra, Jhansirani Jena, Chinmay Kumar Maiti, Strain-Engineering in Nanowire Field-Effect Transistors at 3nm Technology Node, Physica E Low-dimensional Systems and Nanostructures, Elsevier, p. 113964, 2020.
 11. T.P. Dash, J. Jena, E. Mohapatra, **Sanghamitra Das**, S. Dey and C.K. Maiti, Role of stress/strain mapping and random dopant fluctuation in advanced CMOS process technology nodes, International Journal of Nano and Biomaterials, Inderscience, Vol. 9, No. ½, 2020.
 12. E. Mohapatra, R. K. Nanda, **Sanghamitra Das**, T.P. Dash, J. Jena, S. Dey and C.K. Maiti, Strain engineering in AlGaIn/GaN HEMTs for performance enhancement, International Journal of Nano and Biomaterials, Inderscience, Vol. 9, No. ½, 2020
 13. E. Mohapatra, T. P. Dash, J. Jena, **Sanghamitra Das**, C. K. Maiti, "Design study of gate all around vertically stacked nanosheet FETs for sub 7nm nodes," SN Applied Sciences (2021) 3:540
 14. T. P. Dash, J. Jena, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Stress-induced Variability Studies in Tri-Gate FinFETs with Source/Drain Stressor at 7nm Technology Nodes," Journal of Electronic Materials, vol. 48, pp.5348- 5362, 2019.
 15. J. Jena, T. P. Dash, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Fin Shape Dependence of Electrostatics and Variability in FinFETs," Journal of Electronic Materials, vol. 48, 2019.
 16. S. Dey, J. Jena, E. Mohapatra, T. P. Dash, **Sanghamitra Das** and C. K. Maiti, "Design and Simulation of Vertically-Stacked Nanowire Transistors at 3nm Technology Nodes," Physica Scripta, 2019

ANY OTHER

Book Chapter &

Conferences attended **Conferences:**

1. **Sanghamitra Das**, A. Raju and T. P. Dash, "GeometryDependent RF Performance of FinFETs," 2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT), 2021, pp. 1-4, doi: 10.1109/APSIT52773.2021.9641234.
2. **Sanghamitra Das**, E. Mohapatra, S. Choudhury, T. P. Dash and C. K. Maiti, "Stress-EngineeredAlGaN/GaN High Electron Mobility Transistors Design," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 471-473, doi: 10.1109/DevIC50843.2021.9455852.
3. J. Jena, **Sanghamitra Das**, E. Mohapatra, J. Nanda and T. P. Dash, "Performance Analysis of FinFET basedinverterat 7nm TechnologyNodeUsing TCAD Simulation," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 143-147, doi: 10.1109/DevIC50843.2021.9455817.
4. E. Mohapatra, T. P. Dash, **Sanghamitra Das**, J. Jena, J. Nanda and C. K. Maiti, "Investigation of WorkFunction Variation on the Electrical Performance of sub-7nm GAA FETs," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 103-106, doi: 10.1109/DevIC50843.2021.9455911.
5. **Sanghamitra Das**, T. P. Dash, S. Dey, E. Mohapatra, J. R. Jena, and C. K. Maiti, "NBTI Degradation and Recovery in NanowireFETs," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp. 70-74, 2019.
6. T. P. Dash, **Sanghamitra Das**, S. Dey, E. Mohapatra, J. Jena, and C. K. Maiti, "SPICE Parameter Extraction of Tri-GateFinFETs- An IntegratedApproach," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp. 291-294,2019.
7. E. Mohapatra, **Sanghamitra Das**, T. P. Dash, S. Dey, J. Jena and C. K. Maiti, "High Frequency Performance of AlGaN/GaN HEMTsFabricated on SiC Substrates", in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp. 326-330, 2019.
8. E. Mohapatra, **Sanghamitra Das**, T. P. Dash, S. Dey, J. Jena, and C. K. Maiti, "Strain Engineering in AlGaN/GaN HEMTs for Performance Enhancement," 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), IIT Hyderabad, India. February 25-27, 2019.
9. S. Dey, E. Mohapatra, J. Jena, **Sanghamitra Das**, T. P. Dash, and C. K. Maiti, "Performance Prediction of StackedNanowire Transistors in the Presence of RandomDiscrete Dopants and MetalGateGranularity," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp.65-69, 2019.
10. T. P. Dash, S. Dey, E. Mohapatra, **Sanghamitra Das**, J. Jena, and C. K. Maiti, "Vertically-StackedSiliconNanosheet Field Effect Transistors at 3nm TechnologyNodes" , in IEEE International Conference on DeviceIntegrated Circuits (DevIC- 2019), pp. 99-103,2019.
11. T. P. Dash, S. Dey, J. Jena, **Sanghamitra Das**, E. Mohapatra, and C. K. Maiti, "Metal Grain GranularityInducedVariability in Gate-All-Around Si-Nanowire Transistors at 1nm TechnologyNode," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp. 286-290, 2019.
12. T. P. Dash, J. Jena, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Role of stress/StrainMapping in Advanced CMOS ProcessTechnologyNodes," in IEEE International Conference on DeviceIntegrated Circuits (DevIC- 2019), pp. 21-25, 2019.

13. S. Dey, T. P. Dash, E. Mohapatra, J. Jena, **Sanghamitra Das**, and C. K. Maiti, "Performance and Opportunities of Gate-All-Around Vertically-Stacked Nanowire Transistors at 3nm Technology Nodes," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 65-69, 2019.
14. T. P. Dash ; **Sanghamitra Das**; S. Dey ; J. Jena ; E. Mohapatra ; C. K. Maiti, Stress analysis in uniaxially strained-SiGe channel FinFET at 7N Tech. node, 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 24-11-18 to 25-11-18, pp. 171- 175, July, 2019.
15. T. P. Dash; S. Dey ; **Sanghamitra Das**; E. Mohapatra ; J. Jena ; C. K. Maiti, Stress tuning in nanoscale FinFETs at 7nm, 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 24-11-18 to 25-11-18, pp. 166-170, July, 2019
16. S. Dey, J. Jena, T. P. Dash, E. Mohapatra, **Sanghamitra Das** and C. K. Maiti, "Performance Evaluation of Gate-All-Around Si Nanowire Transistors with SiGe Strain engineering," 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), Hyderabad, India, 2019, pp. 29-33.
17. **Sanghamitra Das**, T.P. Dash, R.K. Nanda and C.K. Maiti, Study of Strained-Si/SiGe Channel p-MOSFETs Using TCAD. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing & Communication Systems. Lecture Notes in Electrical Engineering, vol. 453, pp.181-188, Springer, Singapore, 2018.
18. **Sanghamitra Das**, T. P. Dash, S. Dey and C. K. Maiti, "Effects of Trap Position and Number Dependence of Threshold Voltage in p-MOSFETs," 2018 IEEE International Symposium on Devices, Circuits and Systems, 2018.
19. **Sanghamitra Das**, T. P. Dash and C. K. Maiti "Low Frequency Noise analysis in strained-Si Devices," International Conference on Emerging Technology in Modelling and Graphics, India, 2018.
20. T. P. Dash, **Sanghamitra Das** and R.K. Nanda, Silicon-Germanium Channel Heterostructure p-MOSFETs. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing & Communication Systems. Lecture Notes in Electrical Engineering, vol. 453, pp. 365-374, Springer, Singapore, 2018.
21. C. K. Maiti, **Sanghamitra Das** and T. P. Dash, "Technology CAD Simulations of Hot-Carrier Degradation in Strained-Si p-MOSFETs" ", in IEEE International Conference on Device Integrated Circuits (DevIC-2017), 23-24 March, 2017.
22. T. P. Dash, **Sanghamitra Das** and D. Pradhan, "Low Temperature Simulation of Strained-Si n-MOSFETs," in International Conference on Smart Materials & Applications (ISMA-2016), 2016.
23. D. Pradhan, **Sanghamitra Das** and T. P. Dash, "Effect of temperature and scaling on the behavior of strained Si p-MOSFETs ", 3rd International Conference on Electrical, Electronics, Engineering trends, Communication, Optimization and Sciences (EEECOS)-2016, 1-2 June, 2016.
24. T. P. Dash, D. Pradhan, **Sanghamitra Das** and R. K. Nanda, "Electron mobility modeling in strained-Si n-MOSFETs using TCAD," in 13th IEEE India Conference INDICON-2016, 16-18 Dec, 2016.
25. **Sanghamitra Das**, R. K. Nanda, T. P. Dash and C. K. Maiti, "Low-Temperature Simulation of strained-Si Channel p-MOSFETs", in 18th

- International Workshop on Physics of Semiconductor Devices (IWPSD-2015), 7th -10th Dec, p. 329, 2015.
26. R.K. Nanda, T. P. Dash, **Sanghamitra Das** and C. K. Maiti, "Beyondsilicon: Strained-SiGe channelFinFETs," in Proceedings - 2015 International Conference on Man and Machine Interfacing, MAMI 2015, art. no. 7456578, 2015.
 27. R. K. Nanda, T. P. Dash, **Sanghamitra Das** and C. K. Maiti, "Noise characterization of Silicon-Germanium HBTs," (2015) in 2015 International Conference on Microwave, Optical and Communication Engineering, ICMOCE 2015, art. no. 7489747, pp. 284-287, 2015.
 28. T. P. Dash, R. K. Nanda, **Sanghamitra Das** and C. K. Maiti. "Technology CAD of Dual Channel Heterostructure MOSFETs," in 18th International Workshop on Physics of Semiconductor Devices (IWPSD-2015), 7th -10th Dec, p.378, 2015.

Patents :

1. Application Number :202131048431

Title of Invention : Monitoring and Control of PVsystemsconnected to the gridwith a conventionalinverter and with an interlacedinverter.

Date of publication : 12-11-2021

2. Application Number :202131050907

Title of Invention :Monitoring And Evaluating The Operation Of Electronic Noses.

Date of publication: 10-12-2021