# Sudhansu Kumar Pati, Ph.D.

**Designation:** Addl. Professor

**Department:** Department of Electronics and Communication Engineering

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## RESEARCH INTERESTS

- ✓ The researchinterests are in the field of Semiconductordevicesthrough Modeling and Simulation.
- ✓ Mainlyfocussed on the Physics and the characterization of Metal-Oxide-Semiconductor (MOS) Field-Effect-Transistors, High speed Electron Mobility Transistors (HEMT) and MOS-HEMT devices.
- ✓ Investigating the new channelmaterial of the MOS device structures to overcome the shortfall of performances in the new trend technology.
- ✓ To explore the new CMOS structures to fit in SoC fabrication by the Noise and RF analysis.

## Academic Qualifications

Ph. D. (ECE), Jadavpur University, Kolkata, India

M. Tech. (EE), NIT Rourkela, Odisha, India

Specialisation: Electronic Systems & Communication

## Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching experience-16 years
- ✓ Research experience-9 years

## PUBLICATIONS

### JOURNAL& CONFERENCES

1. **Sudhansu Kumar Pati**, HemantPardeshi, Godwin Raj, N. Mohankumar and Chandan Kumar Sarkar, "Flicker and thermal noise in an n-channel underlap DG FinFET in a weak inversion region", Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-6, February 2013. ISSN:1674-4926, DOI: 10.1088/1674-4926/34/2/024002, (SCI-Impact factor 1.18)
2. **Sudhansu Kumar Pati**, HemantPardeshi, Godwin Raj, N. Mohankumar and Chandan Kumar Sarkar, "Impact of gate length and barrier thickness on performance of InP/InGaAs based Double

Gate Metal–Oxide-Semiconductor Heterostructure Field-Effect Transistor (DG MOS-HFET)", Superlattices and Microstructures - ELSEVIER Publishers,Vol. 55, Pages:8–15, 2013. ISSN: 0749-6036, DOI: 10.1016/j.spmi.2012.12.002 (SCI-Impact factor 2.12)

3. **Sudhansu Kumar Pati**, KalyanKoley, ArkaDutta, N. Mohankumar and Chandan Kumar Sarkar," A New Approach to Extract the RF Parameters of Asymmetric DG MOSFET with NQS Effect", Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-5, November 2013. ISSN:1674-4926, DOI: 10.1088/1674-4926/34/11/114002 (SCI-Impact factor 1.18)
4. **Sudhansu Kumar Pati**, KalyanKoley, ArkaDutta, N. Mohankumar and Chandan Kumar Sarkar," Study of body and oxide thickness variation on analog and RF performance of underlap DG-MOSFETs", Microelectronics Reliability-Elsevier Publishers,Vol. 54, No. 6–7, Pages: 1137–1142, 2014. ISSN: 0026-2714, DOI: 10.1016/j.microrel.2014.02.008
5. HemantPardeshi, **Sudhansu Kumar Pati**, Godwin Raj, N. Mohankumar and Chandan Kumar Sarkar," Effect of underlap and gate length on device performance of an AlInN/GaN underlap MOSFET", Journal of Semiconductors, IOP Science publishers, Vol. 33, No. 12, pp. 1-7, 2012. ISSN:1674-4926, DOI: 10.1088/1674-4926/33/12/124001(SCI-Impact factor 1.18)
6. HemantPardeshi, **Sudhansu Kumar Pati**, Godwin Raj, N. Mohankumar and Chandan Kumar Sarkar, "Investigation of asymmetric effects due to gate misalignment, gate bias and underlap length in III–V heterostructure underlap DG MOSFET", Physica E: Low-dimensional Systems and Nanostructures, Elsevier, Vol. 46, pp. 61–67, 2012. ISSN: 1386-9477, DOI: 10.1016/j.physe.2012.09.011(SCI-Impact factor 3.57)
7. HemantPardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohankumar and Chandan Kumar Sarkar, "Comparative Assessment of III–V Heterostructure and Silicon Underlap Double Gate MOSFETs", Semiconductors, Springer, Vol. 46, No. 10, pp. 1299–1303, 2012. ISSN: 1090-6479, DOI: 10.1134/S1063782612100119 (SCI-Impact factor 0.641)
8. Godwin Raj, HemantPardeshi, **Sudhansu Kumar Pati**, N. Mohankumar and Chandan Kumar Sarkar," Physics Based Charge and Drain Current Model for AlGaN/GaN HEMT Devices", Journal of Electron Devices, Vol. 14, pp. 1155-1160, 2012. ISSN: 1682-3427
9. Godwin Raj, HemantPardeshi, **Sudhansu Kumar Pati**, N. Mohankumar and Chandan Kumar Sarkar," Polarization based charge density drain current and small-signal model for nano-scale AlInGaN/AlN/GaN HEMT devices", Superlattices and Microstructures, Elsevier, Vol. 54, pp. 188–203, 2013. ISSN: 0749-6036, DOI: 10.1016/j.spmi.2012.11.020(SCI-Impact factor 2.12)
10. HemantPardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohankumar and Chandan Kumar Sarkar," Influence of barrier thickness on AlInN/GaN underlap DG MOSFET device performance", Superlattices and Microstructures, Elsevier, Vol. 60, pp. 47–59, 2013. ISSN: 0749-6036, DOI: 10.1016/j.spmi.2013.04.015(SCI-Impact factor 2.12)

11. HemantPardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohankumar and Chandan Kumar Sarkar," Performance assessment of gate material engineered AlInN/GaN underlap DG MOSFET for enhanced carrier transport efficiency", Superlattices and Microstructures, Elsevier, Vol. 60, pp. 10–22, 2013. ISSN: 0749-6036, DOI: 10.1016/j.spmi.2013.04.019 (SCI-Impact factor 2.12)
12. Sanjit Kumar Swain, Sarosij Adak, **Sudhansu Kumar Pati**, HemantPardeshi and Chandan Kumar Sarkar," Analysis of flicker and thermal noise in p-channel Underlap DG FinFET", Microelectronics Reliability, Elsevier, Vol. 54, No. 8, pp. 1549–1554, 2014. ISSN: 0026-2714, DOI: 10.1016/j.microrel.2014.04.002(SCI-Impact factor 1.535)
13. Sarosij Adak, Sanjit Kumar Swain, Avtar Singh, HemantPardeshi, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar," Study of HfAlO/AlGaN/GaN MOS-HEMT with source field plate structure for improved breakdown voltage", Physica E: Low-dimensional Systems and Nanostructures, Elsevier, Vol. 64, pp. 152–157, 2014. ISSN: 1386-9477, DOI: 10.1016/j.physe.2014.07.021(SCI-Impact factor 3.57)
14. Sarosij Adak, ArghyadeepSarkar, Sanjit Swain, HemantPardeshi, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "High Performance AlInN/AlN/GaN p-GaN Back Barrier Gate-Recessed Enhancement-Mode HEMT", Superlattices and Microstructures, Elsevier, Vol. 75, pp. 347–357, 2014. ISSN: 0749-6036, DOI:10.1016/j.spmi.2014.07.036 (SCI-Impact factor 2.12)
15. Sanjit Kumar Swain, Sarosij Adak, Bikash Sharma, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Effect of Channel Thickness and Doping Concentration on Sub-Threshold Performance of Graded Channel and Gate Stack DG MOSFETs", Journal of Low Power Electronics, American Scientific Publishers, Vol. 11, pp. 366-372, 2015, ISSN:1546-1998 DOI: 10.1166/jolpe.2015.1395
16. Sanjit Kumar Swain, ArkaDutta, Sarosij Adak, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Influence of channel length and high-K oxide thickness on subthreshold analog/RF performance of graded channel and gate stack DG-MOSFETs", Microelectronics Reliability, Elsevier, Vol. 61, pp. 24-29, 2016, . ISSN: 0026-2714, DOI:10.1016/j.microrel.2016.03.001 (SCI-Impact factor 1.535)
17. Sanjit Kumar Swain, Sarosij Adak, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Impact of InGaN back barrier layer on performance of AlInN/AlN/GaN MOS-HEMTs", Superlattices and Microstructures, Elsevier, Vol. 97, pp. 258-267, 2016. ISSN: 0749-6036, DOI: 10.1016/j.spmi.2016.06.032 (SCI-Impact factor 2.12)
18. **Sudhansu Kumar Pati**, ArghyadeepSarkar, HemantPardeshi, Godwin Raj, N Mohankumar and Chandan Kumar Sarkar, "Analytical Drain Current Model for Symmetrical Gate Underlap DGMOSFET", IJCA Proceedings on International Conference on Communication, Circuits and Systems 2012 iC3S(3):26-28, June 2013.
19. **Sudhansu Kumar Pati**, HemantPardeshi, Godwin Raj, N Mohankumar and Chandan Kumar Sarkar, "Comparison study of Drain Current, Subthreshold Swing and DIBL of III-V Heterostructure and Silicon Double Gate MOSFET", IJECT ,Vol. 4, Issue spl - 1, Jan - March 2013

20. **Sudhansu Kumar Pati**, HemantPardeshi, Godwin Raj, N Mohankumar and Chandan Kumar Sarkar, "Performance Comparison of III-V Heterostructure and Silicon Double Gate MOSFET", 2nd International Conference on Advances in Engineering and Technology (ICAET2012), March 28 & 29, 2012.
21. SaritaMisra, Sudhanshu Mohan Biswal,BiswajitBaral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, 'Study of Effect of downscaling on the Analog/RF Performance of Gate all Around JLMOSFET' , 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 234-241, DOI:10.1109/EDKCON.2018.8770424, Corpus ID: 198929394
22. Sudhanshu Mohan Biswal,BiswajitBaral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET" 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 344-348, DOI: 10.1109/EDKCON.2018. 8770447

## ANY OTHER

Book Chapter
Conferences attended