Santunu Sarangi, M.tech

Designation : Assistant Professor

Department : Department of Electronics & Communication Engg.
(JOINED THE INSTITUTE IN JANUARY 2019)

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RESEARCH INTERESTS

Analog and Mixed Signal VLSI Design :

- ✓ High-Speed SerDes Design
- ✓ On-Chip Jitter Measurement Circuit Design
- ✓ VCO, PLL and ADC Design
- ✓ Power Management Integrated Circuit Design
- ✓ Custom Analog and RF Layout Design and Iptimization

Academic Qualifications

Ph.D. in High Frequency VLSI Design (Thesis Submitted), IIT Kharagpur
M. Tech in VLSI Design and EmbeddedSystem, NIT Rourkela, Odisha.
B. Tech in Electronics and Telecom. Engg, ITER Bhubaneswar,Odisha.

Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience : 4years
- ✓ Research Experience : 8 years
- ✓ Industry Experience : 7 years

PUBLICATIONS

JOURNAL AND CONFERENCES:
JOURNALS:

1. I. Som, **S. Sarangi** and T. K. Bhattacharyya, "A 7.1-GHz 0.7-mW Programmable Counter With Fast EOC Generation in 65-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 11, pp. 2397-2401, Nov. 2020,
2. **Santunu Sarangi,** Shiv Bhushan, AbirmoyaSantra, SarveshDubey, SatyabrataJit, Pramod Kumar Tiwari, "A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs", Superlattices and Microstructures, Vol. 60, 2013, pp. 263-279.
3. Bhushan, Shiv; **Santunu Sarangi**; Gopi, Krishna Saramekala; Santra, Abirmoya; Dubey, Sarvesh; Tiwari, Pramod Kumar; "An Analytical Model for The Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETS with a Strained-Silicon (S-Si) Channel On Silicon-Germanium

(SiGe) Substrates", Journal of Semiconductor Technology and Science, Volume 13, Issue 4, 2013, Pp.367-380.

4. Shiv Bhushan, **Santunu Sarangi**, AbirmoyaSantra, Mirgender Kumar, SarveshDubey, S. Jit and P. K. Tiwari, "An Analytical Surface Potential Model for Strained-Si On Silicon germanium MOSFET Including the Effects of Interface Charges" Journal of Electron Devices, Vol. 15, 2012, pp. 1285-1290.

CONFERENCES:

1. **Santunu Sarangi**, IndranilSom, and T K Bhattacharyya, "A 10 Gb/s On-chip Jitter Measurement Circuit Based on Transition Region Scanning Method", 35th International Conference on VLSI Design & 21th International Conference on Embedded Systems, VLSID 2022, Feb 26 – Mar 02, 2022. (Conference), accepted and presented.
2. **Santunu Sarangi**, IndranilSom, and T K Bhattacharyya, "A Compact and Low-power TransmitterDriver Design for High-Speed SerDes System", 34th International Conference on VLSI Design & 20th International Conference on Embedded Systems, VLSID 2021, Feb 2020. (Conference), accepted and presented.
3. **Santunu Sarangi,**SubhraSutapaMohapatra, DhananjayaTripathy, and Saroj Rout, "A Power- and Area-Efficient CMOS Bandgap Reference Circuit with an Integrated Voltage-Reference Branch", International conference on Modelling, Simulation and Intelligent Computing, 2020, pp. 144-154.
4. **S. Sarangi,** A. Santra, S. Bhushan, K. S. Gopi, S. Dubey and P. K. Tiwari, "An analytical surface potential modeling of fully-depleted symmetrical double-gate (DG) strained-Si MOSFETs including the effect of interface charges," 2013 Students Conference on Engineering and Systems (SCES), 2013, pp. 1-5, doi: 10.1109/SCES.2013.6547495.
5. **S. Sarangi**, S. Bhushan, S. G. Krishna, A. Santra and P. K. Tiwari, "A simulation-based study of gate misalignment effects in triple-material double-gate (TMDG) MOSFETs," 2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), 2013, pp. 486-489, doi: 10.1109/iMac4s.2013.6526461.ANY Other

PATENTS

1. **Santunu Sarangi,** Indranil Som, and T. K. Bhattacharyya, "On-chip jitter measurement circuit for high speed data and clock", Indian Patent filed, Filing No: 201931004744, Feb 2019
2. Indranil Som, **Santunu Sarangi,** and T. K. Bhattacharyya, "High-speed voltage controlled CML hysteresis delay cell and ring oscillator using the same", Indian Patent filed, Filing No: 201931004949, Feb 2019

INDUSTRY PROJECTS:

1. Standard Cell Library Development in 40nm CMOS Technology for Sevya Multimedia, Greater Noida, New Delhi, India, Aug-Dec, 2019
2. Bandgap Refernce and Current DAC Design in 180 nm CMOS Technology for Boston Micro Technology, USA, March-September, 2020.
3. Development of Ultra-low current reference circuit in 28 nm CMOS Technology for InnateraNanoSystems, Netherland, January-June, 2021.

CONSULTANCY:

1. Working as an Analog and Mixed Signal IP Design Consultant for Sevya Multimedia Pvt Ltd from March, 2020 to Present.
2. Working as an VLSI Design mentor in Sevya-SIT Launch Lab from October 2021 to present.