# Sudhansu Mohan Biswal, Ph.D.


**Designation** : Associate Professor

**Department** : Department of Electronics &Communication Engineering

(JOINED THE INSTITUTE IN JAN2007)

**Contact** : +91-9438788420, 9861863662

**Email** : sudhansu.mohan@silicon.ac.in


## RESEARCH INTERESTS

- ✓ Semiconductor devices modeling and simulation study
- ✓ VLSI Design
- ✓ IoT & Automation Control

## Academic Qualifications

Ph. D. (Engg) Maulana Abul Kalam Azad University of Technology, West Bengal, India

M. Tech. (Electronics &Communication Engg.),BPUT, Odisha

B. Tech. (AE&I), Utkal University, Odisha

Specialisation: Nano Electronics & Device engg.

## Teaching Experience/Industrial Experience/Research Experience

Teaching Experience : More than 18 years

Research Experience : More than 7 years

## PUBLICATIONS

### JOURNAL

1. **Biswal, S.M.**, Baral, B., De, D. and Sarkar, A., "Analytical subthreshold modeling of dual material gate engineered nano-scale junctionless surrounding gate MOSFET considering ECPE" ***Superlattices and Microstructures*, published by Elsevier** B.V., vol. *82*, pp.103-112*.*, 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140
2. **Biswal, S.M.**, Baral, B., De, D. and Sarkar, A., "Study of effect of gate-length downscaling on the analog/RF performance and linearity investigation of InAs-based nanowire Tunnel FET" ***Superlattices and Microstructures*,published by Elsevier** vol. 91, pp. 319-330, 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140
3. **Biswal, S. M.**,Baral, B.*, D.* De, and Sarkar A. "Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET"*Advances in Industrial Engineering and Management*, published by **American Scientific Publishers, USA,** vol. 5, no. 1, pp. 150-156, 2016, DOI: 10.7508/aiem. 2016.01.005.
4. **Biswal, Sudhansu Mohan**, Biswajit Baral, Debashis De, and A. Sarkar. "Simulation and comparative study on analog/RF and linearity performance of III–V semiconductor-based staggered heterojunction and InAs nanowire (nw) Tunnel FET**." *Microsystem Technologies*** (2017)**SPRINGER:** 1-7**Impact factor :1.513**

5. Baral. B.**,Biswal. S,**De. D*, and* Sarkar. A. "Effect of gate-length downscaling on the analog/RF and linearity performance of InAs-based nanowire tunnel FET***"International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,* published by John Wiley & Sons Inc.,** vol. 30, no. 3-4, 2016, doi: 10.1002/jnm.2186,.(**SCI Indexed**) **Impact Factor: 0.833.**
6. Baral, B.*,* **Biswal, S. M**.*,* De, D.*, and* Sarkar A. " RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET" *Simulation: Transactions of the Society for Modeling and Simulation International*" published by **SAGE Publications, United Kingdom,** vol. 1-9, 2017 **(SCI Indexed) Impact Factor: 0.713**
7. Baral, B.*,* **Biswal, S. M**.*,* De, D.*, and* Sarkar A. "Effect of gate length downscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications & it's comparative study with conventional Mosfet"*Advances in Industrial Engineering and Management*, published by **American Scientific Publishers, USA** vol. 5, no. 1, 2016, pp. 130-137, DOI: 10.7508/aiem.2016.01.005.
8. Swain, S., **Biswal, S. M**.*,Das*S.,Adak S.,Baral B. " Performance Comparasion of InAs based DG-MOSFET with respect to SIO2 and Gate stack configuration"**Journal of Nanoscience & Nanotechnology-Asia,published by Betham Science.**Vol.9, 2019**(SCI Indexed) Impact factor : 0.78**
9. Misra,S., **Biswal S.M**.,Baral B.,Swain S.,Sarkar A,Pati S. "Analytical modelling of Cyl-JLAMOSFET in subthreshold region using distinct device geometry"**Journal of Computaional Electronics:SPRINGER Publications,vol1-14, 2020(SCI Indexed) Impact factor:1.86 DOI:**10.1007/s10825-020-01560-z
10. Parija, S.K., Swain, S.K., Adak, S**., Biswal, S.M**. and Dutta, P., 2021. Comparison Study of DG-MOSFET with and without Gate Stack Configuration for BiosensorApplications. **Silicon,Springerpp.1-12.**
11. Das, S.K., Nanda, U., **Biswal, S.M**., Pandey, C.K. and Giri, L.I., 2021. Performance Analysis of Gate-Stack Dual-Material DG MOSFET Using Work-Function Modulation Technique for Lower Technology Nodes. **Silicon**,**Springer** pp.1-9.
12. Misra, S., **Biswal, S.M.**, Baral, B., Swain, S.K. and Pati, S.K., 2021. Study of Analog/Rf and Stability Investigation of Surrounded Gate Junctionless Graded Channel MOSFET (SJLGC MOSFET). **Silicon,Springer pp.1-12.**
13. Parija, S.K., Swain, S.K., **Biswal, S.M**., Adak, S. and Dutta, P., 2022. Performance Analysis of Gate Stack DG-MOSFET for Biosensor Applications. **Silicon,Springer pp.1-9.**
14. Chand, N., Adak, S., Swain, S.K., **Biswal, S.M**. and Sarkar, A., 2022. Performance enhancement of normally off InAlN/AlN/GaN HEMT using aluminium gallium nitride back barrier. **Computers & Electrical Engineering**, **published by Elsevier98, p.107695**.
15. Bhol, K., Nanda, U., Jena, B., Tayal, S. and **Biswal, S.M**., 2022. Development of an analytical model of work function modulated GAA MOSFET for electrostatic performance analysis. **Physica *Scripta*.**
16. Tripathy, D., Acharya, D.P., Rout, P.K. and **Biswal, S.M.**, 2022. INFLUENCE OF OXIDE THICKNESS VARIATION ON ANALOG AND RF PERFORMANCES OF SOI FINFET. **Facta Universitatis, Series: Electronics and Energetics, 35(1), pp.001-011.**
17. **Sudhansu M. Biswal**, Satish K. Das, Sarita Misra, Umakanta Nandaand Biswajit Jena.2021. Study on Analog/RF and Linearity Performance of Staggered Heterojunction Gate Stack Tunnel FET The Electrochemical Society("ECS").**IOPPublishingLimitedECS Journal of Solid State Science and Technology, Volume 10**,

## CONFERENCE

1. **Sudhansu Mohan Biswal**, Biswajit Baral, et al. "Study of effect of gate-length downscaling on the Analog/RF performance of Tunnel FET." International conference Nanocon 014, Pune, 14th&15th October 2014.
2. Biswajit Baral, **Sudhansu M Biswal**, et al. " Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th &15th October 2014
3. **Sudhansu Mohan Biswal**,Biswajit Baral, et al. " Simulation and comparative study on Analog/rF performance of Silicon and InAs nanowire Tunnel FET " TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016), (MAKAUT).
4. **Sudhansu Mohan Biswal**,Biswajit Baral,et al. " Analog/RFand Linearity Performance of staggered heterojunction Nanowire Tunnel FET for low power application." 2nd International conference on Devices for Integrated Circuits(DevIC-2017).
5. **Sudhansu Mohan Biswal**,Biswajit Baral, et al. " Analog/RF performance and linearity investigation of Si-based double gate Tunnel FET " 1st International conference on Devices for Integrated Circuits(DevIC-2016).
6. Biswajit Baral,**Sudhansu Mohan Biswal**, et al. " Performance Investigation of III-V Heterosturucture Underlap Double GateMOSFET for System-On-Chip Application." 2nd International conference on Devices for Integrated Circuits(DevIC-2017).
7. Biswajit Bara**l**, **Sudhansu Mohan Biswal**, et al. "Performance Analysis of Downscaled Triple Material Double Gate Junctionless MOSFET using High-K for Analog/mixed signal System-on-chip Applications." TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016). (MAKAUT)
8. Biswajit Baral,**Sudhansu M Biswal**, et al. " Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th&15th October 2014.Payel Chand,
9. Nikhil Agarwal, Biswajit Baral,**Sudhansu Mohan Biswal**"Comparative Study of Gate Underlap and Overlap in Junction-less DG-MOSFET with High k-Spacer through simulation" National conference on Recent Advances on electrical and electronics engg. (NCRAEEE-15), 27th -28th March,2015, GIFT, Bhubaneswar.
10. B.Baral, P.priya, R.Nayak, S. Pradhan, **S.M.Biswal** "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET"IEEE International Conference on Communication and Electronics System(ICCES-2017),19th-20th October 2017,Coimbatore.
11. B.Baral, **S.M.Biswal,** P.Priya, S.K.Swain, S.Mishra "Impact of variation in barrier thickness on a Gate-Engineered TM-DG Heterostructure MOSFET to suppress SCEs and Analog, RF, Linearity performance investigation for SOC applications" IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.
12. S.K.Swain, S. Adak, **S.M.Biswal**, B.Baral, S.Parija "Comparision of Linearity Performance of InP Based DG MOSFETs with Gate Stack SIO2 and HfO2" IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.
13. **S.M.Biswal**, B.Baral, S.K.Swain, S.K.Pati "Performance Analysis of Down Scaling Effect of Si Based SRG Tunnel FET." IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.

14. S.Mishra, **S.M.Biswal**, B.Baral, S.K.Swain, S.K.Pati "Study of Effect of Down Scaling on the Analog/RF Performance of Gate All Around JL MOSFET." IEEE Electron Device Kolkata Conference, (EDKCON-2018), 24th-25th Nov 2018, Kolkata.
15. B.Baral, P.priya, R.Nayak, S. Pradhan,**S.M.Biswal** "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET"IEEE International Conference on Communication and Electronics System(ICCES-2017),19th-20th October 2017, Coimbatore
16. Swain, Sanjit Kumar, Sarosij Adak, **Sudhansu Mohan Biswal**,Biswajit Baral,and Saradiya Parija. "Comparison of Linearity Performance of InAs Based DG-MOSFETs with Gate Stack, SiO2 and HfO2." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 242-246. IEEE, 2018.
17. Das, Satish Kumar, **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, andBiswajit Baral. "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET." In International Conference on Intelligent Computing and Communication Technologies, pp. 803-812. Springer, Singapore, 2019.
18. **Biswal, Sudhansu Mohan**,Biswajit Baral, Sanjit Kumar Swain, and Sudhansu Kumar Pati. "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET." In 2018 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 344-348. IEEE, 2018.
19. **Biswal, Sudhansu Mohan**, Sanjit Kumar Swain,Biswajit Baral,Debasish Nayak, Umakanta Nanda, Satish Kumar Das &Dhananja Tripthy."Performance Analysis of Staggered Heterojunction based SRG TFET biosensor for health IoT applica-tion." In 2019 Devices for Integrated Circuit (DevIC), pp. 493-496. IEEE, 2019.
20. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, **Sudhansu Mohan Biswal,** Dhananjaya Tripthy, Sanjit Kumar Swain,Biswajit Baral, and Satish Kumar Das. "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination." In 2019 Devices for Integrated Circuit (DevIC), pp. 314-317. IEEE, 2019.
21. Tripathy, Dhananjaya, Debasish Nayak, **Sudhansu Mohan Biswal**, Sanjit Kumar Swain,Biswajit Baral, and Satish Kumar Das. "A Low Power LNA using Current Reused Technique for UWB Application." In 2019 Devices for Integrated Circuit (DevIC), pp. 310-313. IEEE, 2019.
22. Baral, Biswajit, **Sudhansu Mohan Biswal**, Sanjit Swain, Satish Kumar Das, Debasish Nayak, and Dhananjaya Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC pplications." In 2019 Devices for Integrated Circuit (DevIC), pp. 505-509. IEEE, 2019.
23. Das, Satish K., Sanjit K. Swain,**Sudhansu M. Biswal,**Debasish Nayak,Umakanta Nanda,Biswajit Baral, and Dhananjaya Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET."In 2019 Devices for Integrated Circuit (DevIC), pp.365-369. IEEE, 2019.
24. Chand, N., Swain, S.K., **Biswal, S.M**., Sarkar, A. and Adak, S., 2021, May. Comparative study on analog & RF parameter of InAlN/AlN/GaN normally off HEMTs with and without AlGaN Back barrier. In 2021 Devices for Integrated Circuit (DevIC) (pp. 616-620). IEEE.
25. Tripathy, D., Rout, P.K., Nayak, D., **Biswal, S.M**. and Singh, N., 2021, May. The impact of oxide layer width variation on the performance parameters of FinFET. In 2021 Devices for Integrated Circuit (DevIC) (pp. 577-580). IEEE.

26. kumar Das, S., **Biswal, S.M.**, Baral, B. and Giri, L., 2021, December. Performance Analysis of Heterojunction Tunnel FET Biosensor. In 2021 19th OITS International Conference on Information Technology (OCIT) (pp. 433-436). IEEE.

## BOOK CHAPTER

1. **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, Jyoti Ranjan Sahoo, Anupam K. Swain, Kunal Routaray, Umakanta Nanda, Birendra Biswal, "A Comparative Study Of Junctionless Triple-Material Cylindrical Surrounding Gate Tunnel Fet", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 793-801, 03 November 2018.
2. Umakanta Nanda, Debasish Nayak, Sushant Kumar Pattnaik, Sanjit Kumar Swain,**Sudhansu Mohan Biswal**, Birendra Biswal, "Design And Performance Analysis Of Current Starved Voltage Controlled Oscillator", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 235-246, 03 November 2018.
3. Sanjit Kumar Swain, **Sudhansu Mohan Biswal**, Umakanta Nanda, D. Siva Patro, Suraj Kumar Nayak, Birendra Biswal, "Impact Of P-Gan Gate Length On Performance Of Algan/Gan Normally-Off Hemt Devices", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 803-809, 03 November 2018.

## ANY OTHER

## SOFTWARE SKILLS

1. Silvaco
2. TCAD
3. MATLAB
4. Labview
5. Pspise
6. PLC/SCADA