Sanghamitra Das, Ph.D.

Designation : Senior Assistant Professor

Department : Department of Electronics Engineering

(JOINED THE INSTITUTE IN JULY, 2018)

Contact : 9437386488(M)

Email : Sanghamitra.das@silicon.ac.in

RESEARCH INTERESTS

- ✓ Semiconductor Device Modeling
- ✓ Bandgap Engineered Devices
- ✓ Reliability analysis of advanced heterostructure Devices

Academic Qualifications

Ph. D. (Electronics), Siksha „O" Anusandhan (Deemed to beUniversity), India

M. Tech. (VLSI & Embedded System Design), BPUT, Odisha, India

B.Tech (Electronics&Telecommunication Engineering), BPUT, Odisha, India

Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience (7 years)
- ✓ Research experience (10 years)

PUBLICATIONS

JOURNALS :

JOURNALARTICLES & CONFERENCE PAPERS

[1]. D. Jena, **Sanghamitra Das**& T. P. Dash, Design and Simulation of Enhancement-Mode Vertical Superjunction GaN HEMT withImproved Ron and Cut-Off Frequency. IETE Journal of Research, pp.1–9, 2023.

[2]. DevikaJena, **Sanghamitra Das**, BiswajitBaral, EleenaMohapatra and TaraprasannaDash, Linearityimprovement in graded channel AlGaN/GaN HEMTs for high-speed applications, Physica Scripta, Vol. 98, p. 105936, 2023.

[3]. Eleena Mohapatra, Jhansirani Jena, Devika Jena, **Sanghamitra Das**, Tarapra sanna Dash, Workfunctionvariability and inverter design possibility in advancedgate all aroundFETs, Nanomaterials and Energy, Vol. 12, pp.81-89, 2023.

[4]. E. Mohapatra, D. Jena, **Sanghamitra Das**, C.K. Maiti and T. P. Dash, Design and optimization of stress/strain in GAA nanosheet FETs for improvedFOMsat sub-7 nm nodes, Physica Scripta, Vol. 98, p. 065919, 2023.

[5]. J. Jena, D. Jena, E. Mohapatra, **Sanghamitra Das** & T. P. Dash, FinFET-BasedInverter Design and Optimizationat 7 Nm TechnologyNode, Silicon, Vol. 14, pp.10781–10794, 2022.
[6]. P. P. Maiti, AjitDash, S.Guhathakurata, **Sanghamitra Das**, Atanu Bag, T. P.Dash, G Ahmad, C K MAITI & S Mallik, Experimental and simulation study of charge transport mechanism in HfTiOx high-k gate dielectric on SiGe heterolayers, Bull Mater Sci, Vol. 45, 2022.
[7]. **Sanghamitra Das**, Tara Prasanna Dash, Devika Jena, EleenaMohapatra and Chinmay Kumar Maiti, "Strain-engineering in AlGaN/GaN HEMTs: impact of siliconnitride passivation layer on electrical performance," Physica Scripta, Vol. 96, 2021.
[8]. **Sanghamitra Das,** Tara Prasanna Dash, Suprava Dey, Chinmay Kumar Maiti, NBTI Studies in GaAs p-MOSFETs, Test Engineering and Management, Vol. 82, pp. 2384 – 2390, 2020
[9]. **Sanghamitra Das**, S. Dey, T. P. Dash, E. Mohapatra, J. Jena and C. K. Maiti, "Impact of NBTI and Hot Carrier Stress on nanowire Characteristics," Nanomaterials and Energy, vol. 8, pp.1-7, 2019.
[10]. **Sanghamitra Das**, T. P. Dash, S. Dey, R. K. Nanda and C. K. Maiti, "Reliability Studies on Biaxially Tensile Strained-Si Channel p-MOSFETs," International Journal of Microstructure and Materials Properties, vol.14, pp. 28-46, 2019.
[11]. **Sanghamitra Das**, T. P. Dash and C. K. Maiti, "Negative Bias Temperature Instability in Strained-Si MOSFETs," International Journal of Nano and Bio Materials (IJNBM), vol. 7, pp. 299 – 310, 2018.
[12]. **Sanghamitra Das**, T. P. Dash and C. K. Maiti, "Effects of Hot-Carrier Degradation on the Low Frequency Noise in Strained-Si p-MOSFETs," International Journal of Nanoparticle (IJNP), vol.10, pp. 58-76, 2018.
[13]. D. Pradhan, **Sanghamitra Das** and T. P. Dash, "Study of strained-Si p-channel MOSFETs with HfO2 gatedielectric," Superlattices and Microstructures, vol. 98, pp. 203-207, 2016.
[14]. T. P. Dash, **Sanghamitra Das**, S. Dey, and C. K. Maiti, "Electro-Thermal Assessment of Heterojunction Tunnel-FET for Low-Power Digital Circuits," International Journal of Nanoparticle, vol. 11, pp. 154-162, 2019.
[15]. T. P. Dash, S. Dey, **Sanghamitra Das**, J. Jena, E. Mohapatra, and C. K. Maiti, "Performance Comparison of Strained-SiGe and Bulk-Si Channel FinFETsat 7N Technology Node," Journal of Micromechanics and Microengineering, vol. 29, pp. 104001, 2019.
[16]. T. P. Dash, Suprava Dey, **Sanghamitra Das,** Eleena Mohapatra, Jhansirani Jena, Chinmay Kumar Maiti, Strain-Engineering in Nanowire Field-Effect Transistors at 3nm Technology Node, Physica E Low-dimensional Systems and Nanostructures, Elsevier, p. 113964, 2020.
[17]. T.P. Dash, J. Jena, E. Mohapatra, **Sanghamitra Das**, S. Dey and C.K. Maiti, Role of stress/strain mapping and random dopant fluctuation in advanced CMOS process technology nodes, International Journal of Nano and Biomaterials, Inderscience, Vol. 9, No. ½, 2020.
[18]. E. Mohapatra, R. K. Nanda, **Sanghamitra Das**, T.P. Dash, J. Jena, S. Dey and C.K. Maiti, Strain engineering in AlGaN/GaN HEMTs for performance enhancement, International Journal of Nano and Biomaterials, Inderscience, Vol. 9, No. ½, 2020
[19]. E. Mohapatra, T. P. Dash, J. Jena, **Sanghamitra Das**, C. K. Maiti, "Design study of gate all around vertically stacked nanosheet FETs for sub 7nm nodes," SN Applied Sciences (2021) 3:540
[20]. T. P. Dash, J. Jena, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Stress-induced Variability Studies in Tri-Gate FinFET swith Source/Drain Stress or at 7nm Technology Nodes," Journal of ElectronicMaterials, vol. 48, pp.5348- 5362, 2019.

[21]. J. Jena, T. P. Dash, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Fin Shape Dependence of Electrostatics and Variability in FinFETs," Journal of Electronic Materials, vol. 48, 2019.

[22]. S. Dey, J. Jena, E. Mohapatra, T. P. Dash, **Sanghamitra Das**and C. K. Maiti, "Design and Simulation of Vertically-Stacked Nanowire Transistors at 3nm Technology Nodes," Physica Scripta, 2019

CONFERENCES:

[23]. D. Jena, **SanghamitraDas**, A. Tripathy and T. Dash, "Comparative Study of AlGaN/GaN-Based Polarization Junction Super HFET," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 1-6, 2023.

[24]. P. K. Jena, **Sanghamitra Das**, S. Bardhan, S. Misra, B. Baral and S. K. Pati, "LowFrequency Noise Analysis in AlGaN/GaN HEMTs," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, pp. 1-4, 2023.

[25]. E. Mohapatra, D. Jena, **Sanghamitra Das**, J. Jena and T. Dash, "Work-FunctionVariability impact on the performance of VerticallyStacked GAA FETs for sub-7nm Technology Node," *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)*, Kolkata, India, pp. 440-444, 2022.

[26]. D. Jena, **Sanghamitra Das**, E. Mohapatra, S. Choudhury and T. Dash, "Simulation of GaN-Based Polarization Junction Super HFET for Power Electronics Application," *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)*, Kolkata, India, pp. 302-306, 2022.

[27]. D. Jena, **Sanghamitra Das**, E. Mohapatra and T. Dash, "Effect of Nitride Stress on Linearity performance of AlGaN/GaN HEMT," *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)*, Kolkata, India, pp. 115-118, 2022.

[28]. **Sanghamitra Das**, A. Raju and T. P. Dash, "GeometryDependent RF Performance of FinFETs," 2021 International Conference in Advances in Power, Signal, and Information Technology (APSIT), 2021, pp. 1-4, doi: 10.1109/APSIT52773.2021.9641234.

[29]. **Sanghamitra Das**, E. Mohapatra, S. Choudhury, T. P. Dash and C. K. Maiti, "Stress-Engineered AlGaN/GaN High Electron Mobility Transistors Design," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 471-473, doi: 10.1109/DevIC50843.2021.9455852.

[30]. J. Jena, **Sanghamitra Das**, E. Mohapatra, J. Nanda and T. P. Dash, "Performance Analysis of FinFET based inverter at 7nm Technology Node Using TCAD Simulation," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 143-147, doi: 10.1109/DevIC50843.2021.9455817.

[31]. E. Mohapatra, T. P. Dash, **Sanghamitra Das**, J. Jena, J. Nanda and C. K. Maiti, "Investigation of Work Function Variation on the Electrical Performance of sub-7nm GAA FETs," *2021 Devices for Integrated Circuit (DevIC)*, 2021, pp. 103-106, doi: 10.1109/DevIC50843.2021.9455911.

[32]. **Sanghamitra Das**, T. P. Dash, S. Dey, E. Mohapatra, J. R. Jena, and C. K. Maiti, "NBTI Degradation and Recovery in NanowireFETs," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 70-74, 2019.

[33]. T. P. Dash, **Sanghamitra Das**, S. Dey, E. Mohapatra, J. Jena, and C. K. Maiti, "SPICE Parameter Extraction of Tri-GateFinFETs- An Integrated Approach," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 291-294,2019.

[34]. E. Mohapatra, **Sanghamitra Das**, T. P. Dash, S. Dey, J. Jena and C. K. Maiti, "High Frequency Performance of AlGaN/GaN HEMTs Fabricated on SiC Substrates", in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 326-330, 2019.

[35]. E. Mohapatra, **Sanghamitra Das**, T. P. Dash, S. Dey, J. Jena, and C. K. Maiti, "Strain Engineering in AlGaN/GaN HEMTs for Performance Enhancement," 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), IIT Hyderabad, India. February 25-27, 2019.

[36]. S. Dey, E. Mohapatra, J. Jena, **Sanghamitra Das**, T. P. Dash, and C. K. Maiti, "Performance Prediction of Stacked Nanowire Transistors in the Presence of Random Discrete Dopants and Metal Gate Granularity," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp.65-69, 2019.

[37]. T. P. Dash, S. Dey, E. Mohapatra, **Sanghamitra Das**, J. Jena, and C. K. Maiti, "Vertically-Stacked Silicon Nanosheet Field Effect Transistors at 3nm Technology Nodes" , in IEEE International Conference on Device Integrated Circuits (DevIC- 2019), pp. 99-103,2019.

[38]. T. P. Dash, S. Dey, J. Jena, **Sanghamitra Das**, E. Mohapatra, and C. K. Maiti, "Metal Grain Granularity Induced Variability in Gate-All-Around Si-Nanowire Transistors at 1nm Technology Node," in IEEE International Conference on DeviceIntegrated Circuits (DevIC-2019), pp. 286-290, 2019.

[39]. T. P. Dash, J. Jena, E. Mohapatra, S. Dey, **Sanghamitra Das**, and C. K. Maiti, "Role of stress/StrainMapping in Advanced CMOS Process Technology Nodes," in IEEE International Conference on Device Integrated Circuits (DevIC- 2019), pp. 21-25, 2019.

[40]. S. Dey, T. P. Dash, E. Mohapatra, J. Jena, **Sanghamitra Das**, and C. K. Maiti, "Performance and Opportunities of Gate-All-Around Vertically-Stacked Nanowire Transistors at 3nm Technology Nodes," in IEEE International Conference on Device Integrated Circuits (DevIC-2019), pp. 65-69, 2019.

[41]. T. P. Dash ; **Sanghamitra Das**; S. Dey ; J. Jena ; E. Mohapatra ; C. K. Maiti, Stress analysis in uniaxially strained-SiGe channel FinFET at 7N Tech. node, 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 24-11-18 to 25-11-18, pp. 171- 175, July, 2019.

[42]. T. P. Dash; S. Dey ; **Sanghamitra Das**; E. Mohaptra ; J. Jena ; C. K. Maiti, Stress tuning in nanoscale FinFETsat 7nm, 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 24-11-18 to 25-11-18, pp. 166-170, July, 2019

[43]. S. Dey, J. Jena, T. P. Dash, E. Mohapatra, **Sanghamitra Das**and C. K. Maiti, "Performance Evaluation of Gate-All-Around Si Nanowire Transistors with SiGe Strain engineering," 2019 IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), Hyderabad, India, 2019, pp. 29-33.

[44]. **Sanghamitra Das**, T.P. Dash, R.K. Nanda and C.K. Maiti, Study of Strained-Si/SiGe Channel p-MOSFETs Using TCAD. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing& Communication Systems. Lecture Notes in Electrical Engineering, vol. 453, pp.181-188, Springer, Singapore, 2018.

[45]. **Sanghamitra Das**, T. P. Dash, S. Dey and C. K. Maiti, "Effects of Trap Position and Number Dependence of Threshold Voltage in p-MOSFETs," 2018 IEEE International Symposium on Devices, Circuits and Systems, 2018.

[46]. **Sanghamitra Das**, T. P. Dash and C. K. Maiti "LowFrequency Noise analysis in strained-Si Devices," International Conference on Emerging Technology in Modelling and Graphics, India, 2018.

[47]. T. P. Dash, **Sanghamitra Das**and R.K. Nanda, Silicon–Germanium Channel Heterostructure p-MOSFETs. In: Nath V. (eds) Proceedings of the International Conference on Microelectronics, Computing & Communication Systems. Lecture Notes in Electrical Engineering, vol. 453, pp. 365-374, Springer, Singapore, 2018.

[48]. C. K. Maiti, **Sanghamitra Das** and T. P. Dash, "Technology CAD Simulations of Hot-Carrier Degradation in Strained-Si p-MOSFETs" ", in IEEE International Conference on Device Integrated Circuits (DevIC-2017), 23-24 March, 2017.

[49]. T. P. Dash, **Sanghamitra Das** and D. Pradhan, "Low Temperature Simulation of Strained-Si n-MOSFETs," in International Conference on Smart Materials& Applications (ISMA-2016), 2016.

[50]. D. Pradhan, **Sanghamitra Das**and T. P. Dash, "Effect of temperature and scaling on the behavior of strained Si p-MOSFETs", 3rd International Conference on Electrical, Electronics, Engineering trends, Communication, Optimization and Sciences (EEECOS)-2016, 1-2 June, 2016.

[51]. T. P. Dash, D. Pradhan, **Sanghamitra Das**and R. K. Nanda, "Electron mobilitymodeling in strained-Si n-MOSFETsusing TCAD," in 13th IEEE IndiaConference INDICON-2016, 16-18 Dec, 2016.

[52]. **Sanghamitra Das**, R. K. Nanda, T. P. Dash and C. K. Maiti, "Low-Temperature Simulation of strained-Si Channel p-MOSFETs", in 18th International Workshop on Physics of Semiconductor Devices (IWPSD-2015), 7th -10th Dec, p. 329, 2015.

[53]. R.K. Nanda, T. P. Dash, **Sanghamitra Das**and C. K. Maiti, "Beyond silicon: Strained-SiGe channel FinFETs," in Proceedings - 2015 International Conference on Man and Machine Interfacing, MAMI 2015, art. no. 7456578, 2015.

[54]. R. K. Nanda, T. P. Dash, **Sanghamitra Das**and C. K. Maiti, "Noise characterization of Silicon-Germanium HBTs,"(2015) in 2015 International Conference on Microwave, Optical and Communication Engineering, ICMOCE 2015, art. no. 7489747, pp. 284-287, 2015.

[55]. T. P. Dash, R. K. Nanda, **Sanghamitra Das**and C. K. Maiti. "Technology CAD of Dual Channel Heterostructure MOSFETs," in 18th International Workshop on Physics of Semiconductor Devices (IWPSD-2015), 7th -10th Dec, p.378, 2015.

ANY OTHER

BOOK CHAPTERS

1. **Sanghamitra Das**, Taraprasanna Dash, Biswajit Baral, Sudhansu Mohan Biswal, Devika Jena and Eleena Mohapatra. "Analytical modelling of nanoscale advance devices and their reliability aspects." Nanoelectronics: Physics, Materials and Devices, Elsevier, January 2023, pp.385-408, 10.1016/B978-0-323-91832-9.00011-7, ISBN: 978-0-323-91832-9.
2. **Sanghamitra Das**. "Stress Generation Techniques in CMOS Technology." Stress and Strain Engineering at Nanoscale in Semiconductor Devices, CRC Press, May 2021, www.routledge.com/Stress-and-Strain-Engineering-at-Nanoscale-in-Semiconductor-Devices/Maiti/p/book/9780367519292, ISBN 9780367519292

PATENTS

3. Application Number : 202131048431
   Title of Invention : Monitoring and Control of PV systems connected to the grid with a conventional inverter and with an interlaced inverter.
   Date of publication : 12-11-2021

4. Application Number : 202131050907
   Title of Invention : Monitoring And Evaluating The Operation Of Electronic Noses.
   Date of publication: 10-12-2021