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**Designation** : Additional Professor

**Department:** Department of Electronics Engineering  
(JOINED THE INSTITUTE IN YEAR-2007)

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### RESEARCH INTERESTS

Analysis & characterization of sub micron and deep submicron field effect devices. It includes mathematical analysis and RF analysis of Advanced MOSFETs. Study of wideband gap compound semiconductor based AlGa<sub>N</sub>/Ga<sub>N</sub> MOSHEMT, InAlN/Ga<sub>N</sub> HEMT and MOSHEMT.

Rf & analog performance analysis of double gate nano MOSFETs. Mathematical modeling of different types of noises in underlap double gate MOSFETs. Several structural optimization of Ga<sub>N</sub> based devices for better performance.

**Academic Qualifications** – Ph.D. in Engineering  
(Jadavpur University, Kolkata)

### Teaching Experience/Industrial Experience/Research Experience

- ✓ 20 years of Teaching experience includes 3 years of Research and 6 months of Industry experiences.

## PUBLICATIONS

### JOURNAL & CONFERENCES

- [1]. High performance AlInN/AlN/GaN p-GaN Back Barrier Gate-Recessed Enhancement-Mode HEMT; Sarosij Adak, Arghyadeep Sarkar, Sanjit Swain, Hemant Pardeshi, Sudhansu Kumar Pati, Chandan Kumar Sarkar; *Superlattices and Microstructure* (Elsevier), 2014, 75, 347–357. Impact Factor 2.12
- [2]. Study of HfAlO/AlGa<sub>N</sub>/Ga<sub>N</sub> MOS-HEMT with source field plate structure for improved breakdown voltage; Sarosij Adak, **Sanjit Kumar Swain**, Avtar Singh, Hemant Pardeshi, Sudhansu Kumar Pati, Chandan Kumar Sarkar; *Physica E: Low-dimensional Systems and Nanostructures* (Elsevier), 2014, 64, 152–157. Impact Factor 2.22

- [3]. Impact of gate engineering in enhancement mode  $n^{++}\text{GaN}/\text{InAlN}/\text{AlN}/\text{GaN}$  HEMTs; Sarosij Adak, **Sanjit Kumar Swain**, Hafizur Rahaman, Chandan Kumar Sarkar; **Superlattices and Microstructure (Elsevier)**, 2016,100, 306-314. Impact Factor 2.12
- [4]. Effect of Barrier Thickness on Linearity of Underlap  $\text{AlInN}/\text{GaN}$  DG-MOSHEMTs; Sarosij Adak, **Sanjit Kumar Swain**, Hemant Pardeshi, Hafizur Rahaman, Chandan Kumar Sarkar; **NANO: Brief Reports and Reviews (World Scientific Publishing Company)**; 2017,12, (01), 1750009. Impact Factor 1.26
- [5]. Influence of Channel length and High-K oxide Thickness on Subthreshold DC Performance of Graded Channel and Gate stack DG-MOSFETs; Sarosij Adak, **Sanjit Kumar Swain**, Arka Dutta, Hafizur Rahaman, Chandan Kumar Sarkar; **NANO: Brief Reports and Reviews (World Scientific Publishing Company)** 2016, 11, (09), and 1650101. Impact Factor 1.26
- [6]. Analysis of flicker and thermal noise in p-channel Underlap DG FinFET; **Sanjit Kumar Swain**, Sarosij Adak, Sudhansu Kumar Pati, Hemant Pardeshi, Chandan Kumar Sarkar; **Microelectronics Reliability (Elsevier)**; 2014, 54 (8), 26, 1549–1554. Impact Factor 1.37
- [7]. Effect of Channel Thickness and Doping Concentration on Sub-Threshold Performance of Graded Channel and Gate Stack DG MOSFETs; **Sanjit Kumar Swain**, Sarosij Adak, Bikash Sharma, Sudhansu Kumar Pati, Chandan Kumar Sarkar; **Journal of Low Power Electronics (American Scientific Publishers)**; 2015, 11(10),1-7. Impact Factor 0.84
- [8]. Influence of channel length and high-K oxide thickness on subthreshold analog/RF performance of graded channel and gate stack DG-MOSFETs; **Sanjit Kumar Swain**, Arka Dutta, Sarosij Adak, Sudhansu Kumar Pati, Chandan Kumar Sarkar; **Microelectronics Reliability (Elsevier)**; 2016, 61, 24-29. Impact Factor 1.37
- [9]. Impact of InGaN back barrier layer on performance of  $\text{AlInN}/\text{AlN}/\text{GaN}$  MOS-HEMTs; **Sanjit Kumar Swain**, Sarosij Adak, Sudhansu Kumar Pati, Chandan Kumar Sarkar; **Superlattices and Microstructure (Elsevier)**, 2016, 97(20) , 258–267. Impact Factor 2.12
- [10]. Performance study of GCGS DG-MOSFETs for Asymmetric Doping and High K Oxide Material Using NQS Method. **Sanjit Kumar Swain**, Sarosij Adak, Saradiya Parija, Chandan Kumar Sarkar, **J. of Active and Passive Electronic Devices, Vol. 00, pp. 1–15, 2017-18(Old City Publishing).(ESCI)**
- [11]. Impact of high-K dielectric materials on performance analysis of underlap  $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaNDG}$ -MOSHEMTs. **Sanjit Kumar Swain**, Sarosij Adak. **NANO: Brief Reports and Reviews (World Scientific Publishing Company)(SCI)**
- [12]. Study of Linearity Performance of Graded Channel Gate Stacks Double Gate MOSFET with Respect to High-K Oxide Thickness. **Sanjit Kumar Swain**, Satish Kumar Das, Sarosij Adak. Silicon(Springer Publication),2019.**SCI**
- [13]. Performance Comparison of InAs Based DG-MOSFET with Respect to  $\text{SiO}_2$  and Gate Stack Configuration. **Sanjit Kumar Swain**, Sudhansu Mohan Biswal, Satish Kumar Das, Sarosij Adak , Biswajit Baral. Nanoscience and Nano Technology,2019,**SCI**.

- [14]. Analytical modelling of a Cyl-JLAM MOSFET in the subthreshold region using distinct device geometry. Sarita Misra, Sudhansu Mohan Biswal, Biswajit Baral, **Sanjit Kumar Swain**, Angsuman Sarkar, Sudhansu Kumar Pati. Journal of Computational electronics (Springer), 2020. **SCI**.
- [15]. Comparison Study of DG-MOSFET with and without Gate Stack Configuration for Biosensor Applications. Saradiya Kishor Parija, **Sanjit Kumar Swain**, Sarosij Adak, Sudhansu Mohan Biswal, Pradipta Dutta .Silicon (Springer Publication), 2021. **SCI**
- [16]. Performance Analysis of Gate Stack DG-MOSFET for Biosensor Applications. Saradiya Kishor Parija, **Sanjit Kumar Swain**, Sudhansu Mohan Biswal, Sarosij Adak, Pradipta Dutta .Silicon (Springer Publication), 2021. **SCI**
- [17]. Performance enhancement of normally off InAlN/AlN/GaN HEMT using aluminium gallium nitride back barrier. Nisarga Chand, Sarosij Adak, **Sanjit Kumar Swain**. Sudhansu Mohan Biswal, A Sarkar. Computers and Electrical Engineering ( Elsevier), **SCI**

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#### Book Chapter

- [1]. Sarosij Adak, Arghyadeep Sarkar, **Sanjit Kumar Swain**, Nanotechnology Applications in Electron Devices, Nanotechnology: **Synthesis to Applications, 2017 (CRC Press)**.
- [2]. **Sanjit Kumar Swain**, Sudhansu Mohan Biswal, Umakanta Nanda, D. Siva Patro, Suraj Kumar Nayak, Birendra Biswal, "Impact Of P-Gan Gate Length on Performance Of Algan/Gan Normally-Off Hemt Devices", **Springer Book series on Microelectronics, Electromagnetics and Telecommunications**. pp 803-809, 03 November 2018.
- [3]. Umakanta Nanda, Debasish Nayak, Sushant Kumar Pattnaik, **Sanjit Kumar Swain**, Sudhansu Mohan Biswal, Birendra Biswal, "Design And Performance Analysis Of Current Starved Voltage Controlled Oscillator", **Springer Book series on Microelectronics, Electromagnetics and Telecommunications** pp 235-246, 03 November 2018.
- [4]. Sudhansu Mohan Biswal, **Sanjit Kumar Swain**, Jyoti Ranjan Sahoo, Nupam K. Swain, Kunal Routaray, Umakanta Nanda, Birendra Biswal, "A Comparative Study of Junctionless Triple-Material Cylindrical Surrounding Gate Tunnel Fet", **Springer Book series on Microelectronics, Electromagnetics and Telecommunications** pp 793-801, 03 November 2018.
- [5]. **Sanjit Kumar Swain**, Akshaya Kumar Sahu, Microwave Engineering, Engineers' Mind Publication, 2013 (**ISBN: 81-7406-015-4**).
- [6]. **Sanjit Kumar Swain**, Akshaya Kumar Sahu, Satellite Communication Systems, Engineers' Mind Publication, 2013 (**ISBN: 81-7406-014-6**).
- [7]. **Sanjit Kumar Swain**, Durga Prasad Mishra, Wireless Sensor Network, Engineers' Mind Publication, 2013 (**ISBN: 81-7406-013-9**).

## Conferences attended

- [1]. Effect of AlN Spacer Layer Thickness on Device Performance of AlInN/AlN/GaN MOSHEMT; Sarosij Adak, **Sanjit Kumar Swain**, Hemant Pardeshi, Hafizur Rahaman, and Chandan Kumar Sarkar; *International Conference on Computing Communication Control and Automation (ICCUBEA)*; 2015,. 902-905. IEEE, (Best Paper Award)  
  
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<https://patents.google.com/patent/US20170125565A1/en>
- [2]. Performance analysis of gate material engineering in enhancement mode n++ GaN/InAlN/ AlN/GaN HEMTs; Sarosij Adak, **Sanjit Kumar Swain**, Godwin Raj, Hafizur Rahaman, and Chandan Kumar Sarkar; *3rd International Conference on Devices Circuits and Systems (ICDCS)*; 2016, 89-92. IEEE.
- [3]. Impact of high K layer material on Analog/RF performance of forward and reversed Graded channel Gate Stack DG-MOSFETs; **Sanjit Kumar Swain**, Sarosij Adak, Arka Dutta, Godwin Raj, and Chandan Kumar Sarkar; *3rd International Conference on Devices, Circuits and Systems (ICDCS)*; 2016, pp. 98-102. IEEE, 2016.
- [4]. Effect of Doping in p-GaN Gate on DC performances of AlGaIn/GaN Normally-off scaled HFETs; Sarosij Adak, **Sanjit Kumar Swain**, Hafizur Rahaman, Chandan Kumar Sarkar; *2nd international conference on Devices for Integrated Circuit (DevIC)*; pp. 372-375. IEEE, 2017.
- [5]. Sub threshold Analog &RF Parameter extraction of GCGS DG- MOSFETs with High K material using NQS approach; **Sanjit Kumar Swain**, Sarosij Adak, Saradiya Parija, Chandan Kumar Sarkar; *2nd international conference on Devices for Integrated Circuit (DevIC)*; pp. 216-220. IEEE, 2017.
- [6]. Performance analysis of T-Gate Enhancement mode n++GaIn/InAlN/AlN/GaN HEMT; Srishti Srivastava, **Sanjit Kumar Swain**, Chandan Kumar Sarkar, Sarosij Adak, *2016 International Conference on Innovations in information, Embedded and Communication Systems (ICIIECS)*. (IEEE XPLORE, In Press).
- [7]. Microwave characteristics of 100nm AlGaIn back barrier Gate Recessed Enhancement mode InAlN/AlN/GaN HEMT; Srishti Srivastava, **Sanjit Kumar Swain**, Chandan Kumar Sarkar, Sarosij Adak, *2016 International Conference on Innovations in information, Embedded and Communication Systems (ICIIECS)*. (IEEE XPLORE, In Press).
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- [10]. B.Baral, S.M.Biswal, P.Priya, **Sanjit Kumar Swain**, S.Mishra "Impact of variation in barrier thickness on a Gate-Engineered TM-DG Heterostructure MOSFET to suppress SCEs and Analog, RF, Linearity performance investigation for SOC

applications" IEEE Electron Device Kolkata Conference, EDKCON-2018, (IEEE XPLORE In Press) 24<sup>th</sup>-25<sup>th</sup> Nov 2018, Kolkata.

- [11]. S.M.Biswal, B.Baral, **Sanjit Kumar Swain**, S.K.Pati "Performance Analysis of Down Scaling Effect of Si Based SRG Tunnel FET." IEEE Electron Device Kolkata Conference, EDKCON-2018, (IEEE XPLORE in Press) 24<sup>th</sup>-25<sup>th</sup> Nov 2018, Kolkata.
- [12]. S.Mishra, S.M.Biswal, B.Baral, **Sanjit Kumar Swain**, S.K.Pati "Study of Effect of Down Scaling on the Analog/RF Performance of Gate All Around JL MOSFET." IEEE Electron Device Kolkata Conference, EDKCON-2018, (IEEE XPLORE In Press 24<sup>th</sup>-25<sup>th</sup> Nov 2018, Kolkata.
- [13]. Satish Ku Das, **Sanjit Kumar Swain**, B.Baral "Analysis of Junction-less Triple-Material Cylindrical Surrounding Gate MOSFET, I4CD-2018,(Accepted)
- [14]. Satish Ku Das, **Sanjit Kumar Swain**, B.Baral, S.M. Biswal "Effect of High-K Spacers on Performance of Uniformly doped Gate Stack DG-MOSFET", DeviC-2019,IEEE EXPLORE.(Accepted)
- [15]. **Sanjit Kumar Swain**, Satish Ku Das, B.Baral, S.M. Biswal "Effect of High-K Spacers on Performance of Non-Uniformly doped DG-MOSFET", DeviC-2019, IEEE EXPLORE. (Accepted)
- [16]. Debashis Nayak, **Sanjit Kumar Swain**, Satish Ku Das, B.Baral, S.M.Biswal "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination",DeviC-2019, IEEE EXPLORE.(Accepted)
- [17]. Umakanta Nanda, **Sanjit Kumar Swain**, Satish Ku Das, B.Baral, S.M. Biswal "PLL Performance Optimization for Fast Locking Energy Efficiency and Low Noise", DeviC-2019, IEEE EXPLORE.(Accepted)
- [18]. S.M.Biswal, Biswajit Baral, **Sanjit Kumar Swain**, Satish Ku Das, B. Baral, Debashis Nayak "Performance Analysis of Staggered heterojunction based SRG TFET biosensor for health IoT application", DeviC-2019, IEEE EXPLORE.(Accepted)
- [19]. Biswajit Baral, S.M.Biswal, **Sanjit Kumar Swain**, Satish Ku Das, Debashis Nayak "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications", IEEE EXPLORE.(Accepted)
- [20]. Sarosij Adak, Nisarga Chand, **Sanjit Kumar Swain**, Angsuman Sarkar "Effect of AlGaN Back Barrier on InAlN/AlN/GaN E-Mode HEMT" ,DeviC-2019,IEEE EXPLORE.(Accepted)
- [21]. Dhananjaya Tripathy, Debashis Nayak, **Sanjit Kumar Swain**, Satish Kumar Das "A Low Power LNA using Current Reused Technique for UWB Application", DeviC-2019,IEEE EXPLORE.(Accepted)
- [22]. Umakanta Nanda, Debashis Nayak, **Sanjit Kumar Swain**, Satish Kumar Das "Smart Power Theft Detection System", DeviC-2019, IEEE EXPLORE. (Accepted)