



## Santunu Sarangi, Ph.D.

**Designation:** Assistant Professor

**Department:** Department of Electronics Engineering

(JOINED THE INSTITUTE IN 2019)

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### RESEARCH INTERESTS

- ✓ Analog and Mixed Signal IC Design
- ✓ Power Management IC Design
- ✓ High-speed SerDes Design
- ✓ PLL and Data Converters Design
- ✓ Custom Analog and RF Layout Design and Optimization

### Academic Qualifications

- ✓ Ph. D. in High-Frequency VLSI Design, IIT Kharagpur
- ✓ M. Tech in VLSI Design and Embedded System, NIT Rourkela
- ✓ B. Tech in Electronics and Telecom. Engineering, ITER Bhubaneswar

### Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience: 5+ years
- ✓ Research Experience: 11+ years
- ✓ Industry Experience: 9+ years

## PUBLICATIONS

### JOURNALS:

### JOURNALARTICLES & CONFERENCE PAPERS

- [1]. I. Som, **S. Sarangi** and T. K. Bhattacharyya, "A 7.1-GHz 0.7-mW Programmable CounterWithFast EOC Generationin 65-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 11, pp. 2397-2401, Nov. 2020,
- [2]. **Santunu Sarangi**, Shiv Bhushan, AbirmoyaSantra, SarveshDubey, SatyabrataJit, PramodKumarTiwari, "A rigorous simulation basedstudy of gatemisaligmenteffects in gateengineered double-gate (DG) MOSFETs", Superlattices and Microstructures, Vol. 60, 2013, pp. 263-279.
- [3]. Bhushan, Shiv; **Santunu Sarangi**; Gopi, Krishna Saramekala; Santra, Abirmoya; Dubey, Sarvesh; Tiwari, PramodKumar; "An Analytical Model for

The Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETS with a Strained-Silicon (S-Si) Channel On Silicon-Germanium (SiGe) Substrates", Journal of Semiconductor Technology and Science, Volume 13, Issue 4, 2013, Pp.367-380.

- [4]. Shiv Bhushan, **Santunu Sarangi**, AbirmoyaSantra, MirgenderKumar, SarveshDubey, S. Jit and P. K. Tiwari, "An Analytical Surface Potential Model for Strained-Si On Silicon germanium MOSFET Including the Effects of Interface Charges" Journal of Electron Devices, Vol. 15, 2012, pp. 1285-1290.

## CONFERENCES:

- [1]. **S. Sarangi**, I. Som and T. K. Bhattacharyya, "A 10 Gb/s On-chip Jitter Measurement Circuit Based on Transition Region Scanning Method," *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID)*, Bangalore, India, 2022, pp. 44-49, doi: 10.1109/VLSID2022.2022.00021.
- [2]. P. K. Swain, **S. Sarangi** and S. Rout, "A compact SPI-based SRAM in 0.6um CMOS for Low-Power IoT Applications," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 1-6, doi: 10.1109/CCPIS59145.2023.10291287.
- [3]. **S. Sarangi**, S. Bhushan, S. G. Krishna, A. Santra and P. K. Tiwari, "A simulation-based study of gate misalignment effects in triple-material double-gate (TMDG) MOSFETs," *2013 International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s)*, Kottayam, India, 2013, pp. 486-489, doi: 10.1109/iMac4s.2013.6526461.
- [4]. **Santunu Sarangi**, SubhraSutapaMohapatra, DhananjayaTripathy, and SarojRout, "A Power- and Area-Efficient CMOS Bandgap Reference Circuit with an Integrated Voltage-Reference Branch", *International Conference on Modelling, Simulation and Intelligent Computing*, 2020, pp. 144-154.
- [5]. **S. Sarangi**, A. Santra, S. Bhushan, K. S. Gopi, S. Dubey and P. K. Tiwari, "An analytical surface potential modeling of fully-depleted symmetrical double-gate (DG) strained-Si MOSFETs including the effect of interface charges," *2013 Students Conference on Engineering and Systems (SCES)*, 2013, pp. 1-5, doi: 10.1109/SCES.2013.6547495.

## PATENTS:

- [1]. **Santunu Sarangi**, IndranilSom, and T. K. Bhattacharyya, "On-chip jitter measurement circuit for high-speed data and clock", Indian Patent, Patent No. - 532270, Application No. - 201931004744, Grant Date : 9th April 2024.
- [2]. IndranilSom, **Santunu Sarangi**, and T. K. Bhattacharyya, "High-speed voltage controlled current mode logic delay cell", Indian Patent, Patent No. -544348, Application No. -201931004949, Grant Date: 5th July 2024

## ANY OTHER

### **INDUSTRY PROJECTS :**

- [1]. Standard Cell Library Development in 40nm CMOS Technology for Sevyamultimedia, GreaterNoida, New Delhi, India, Aug-Dec, 2019.
- [2]. Bandgap Reference and Current DAC Design in 180 nm CMOS Technology for Boston Micro Technology, USA, March-September, 2020.
- [3]. Development of Ultra-lowcurrentreference circuit in 28 nm CMOS Technology for Innatera Nano Systems, Netherland, January-June, 2021.
- [4]. Development of bandgap voltage reference circuit in Google-Skywater 130nm CMOS technology for VLSI System Design Pvt. Ltd, Bangalore, Sep-Oct, 2021.
- [5]. Worked on an IO design project in 55nm CMOS Technology for Sevyamultimedia, GreaterNoida, New Delhi, India, May-Sep, 2022.
- [6]. Worked on anHBM Phy design Project in CuttingEdge CMOS Technology for Sevyamultimedia, Hyderabad, India, January-June, 2024.

### **INDUSTRY TRAINING :**

- [1]. Trained over 200 industryfreshers in different VLSI domainslike ; Analog Circuit Design, Circuit Characterization, Analog& RF Layout Design, Standard Cell Library Development, PDK Design, and Digital Verificationthrough Advanced VLSI Laboratory.
- [2]. Trainedover 50 participants in the VLSI System Design open conferencethrough open-source tools to design Analog IC.
- [3]. Trained over 50 students of VLSI Expert Pvt. Ltd in the field of Standard Cell Library Development.
- [4]. Trained 7 Advanced VLSI Lab. Practice School (PS) students and place them all in the VLSI industry.

### **CONSULTANCY:**

- [1]. Working as an Analog and Mixed Signal IP Design Consultant for SevyamultimediaPvt Ltd from March 2020 to Present.
- [2]. Working as a VLSI Design mentor in Sevya-SIT LaunchLabfromOctober 2021 toPresent.