Satish Kumar Das, M.Tech

Designation : Assistant Professor

Department : Department of Electronics Engineering

(JOINEDTHEINSTITUTEINJUNE 2018)

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Research Interests

- ✓ Semiconductor devices modeling and simulation study
- ✓ VLSI Design
- ✓ Signal Processing

Academic Qualifications

Ph. D. National Institute of Technology, Goa, India

M.E. (Electronics &Communication Engg.), BIT, Mesra, India

B. Tech. (AE&I), BPUT, Odisha

Specialisation : Nano Electronics & Device Engg.

Teaching Experience/Industrial Experience/Research Experience

Teaching Experience : More than 11 years

Research Experience : More than 8 years

PUBLICATIONS

JOURNAL ARTICLES & CONFERENCE PAPERS

JOURNAL

[1]. Sanjit Kumar Swain, **Satish Kumar Das** and Sarosij Adak, "Study of Linearity Performance of Graded Channel Gate Stacks Double Gate MOSFET with Respect to High-K Oxide Thickness" , **Silicon, Springer**, pp.1-8, August, 2019, **DOI: 10.1007/s12633-019-00257-8**

[2]. **Das, S.K.,** Nanda, U., Biswal, S.M., Pandey, C.K. and Giri, L.I., 2021. Performance Analysis of Gate-Stack Dual-Material DG MOSFET Using Work- Function Modulation Technique for Lower Technology Nodes. **Silicon,Springer** pp.1-9.

[3]. **Satish K. Das**, Sudhansu M. Biswal, Sarita Misra, Umakanta Nanda and Biswajit Jena. 2021. Study on Analog/RF and Linearity Performance of Staggered Heterojunction Gate Stack Tunnel FET The Electrochemical Society ("ECS"). **IOP Publishing Limited ECS Journal of Solid State Science and Technology, Volume10**, **073001.DOI 10.1149/2162-8777/ac0e10.**

[4]. **Das, S.K**., Biswal, S.M., Giri, L.I. and Swain, D., 2024.Thermal influence on performance characteristics of double gate MOSFET biosensors with gate stack configuration. **Discover Applied Sciences (Springer), doi: 10.1007/s42452-024-06055-1.**

[5]. **Das, S.K**., Biswal, S.M**.,** Giri, L.I. and Nanda U.K**., 2024.** Impact of Deep Cryogenic Temperatures on Gate Stack Dual Material DG MOSFET Performance: Analog and RF Analysis. **e-Prime - Advances in Electrical Engineering, Electronics & Energy. https://doi.org/10.1016/j.prime.2024.100725**

CONFERENCE

[1]. Biswal, Sudhansu Mohan, Sanjit Kumar Swain,Biswajit Baral, Debasish Nayak, Umakanta Nanda, **Satish Kumar Das** & Dhananja Tripthy. "Performance Analysis of Staggered Heterojunction based SRGTFET biosensor for health IoT application. "In 2019 Devices for Integrated Circuit (DevIC), pp.493-496. IEEE, 2019.

[2]. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, Sudhansu MohanBiswal**,** Dhananjaya Tripthy, Sanjit Kumar Swain, Biswajit Bara**l**, and **Satish Kumar Das.** "A Novel Driverless SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination. "In 2019 Devices for Integrated Circuit (DevIC), pp.314-317. IEEE, 2019.

[3]. Tripathy, Dhananjaya, Debasish Nayak, Sudhansu Mohan Biswal, Sanjit Kumar Swain, Biswajit Baral, and **Satish Kumar Das**. "A Low Power LNA using Current Reused Technique for UWB Application. "In 2019 Devices for Integrated Circuit (DevIC), pp.310-313. IEEE, 2019.

[4]. Baral, Biswajit, Sudhansu Mohan Biswal, Sanjit Swain, **Satish Kumar Das,** Debasish Nayak and Dhananjaya Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications. "In 2019 Devices for Integrated Circuit (DevIC), pp.505-509. IEEE, 2019.

[5]. **Das, Satish K.,** Sanjit K. Swain, Sudhansu M. Biswal, Debasish Nayak, Umakanta Nanda, Biswajit Baral, and Dhananjaya Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET. "In 2019 Devices for Integrated Circuit (DevIC), pp.365-369. IEEE, 2019.

[6]. **Das, Satish Kumar,** Sudhansu Mohan Biswal, Sanjit Kumar Swain, and Biswajit Baral. "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET. "In International Conference on Intelligent Computing and Communication Technologies, pp.803-812. Springer, Singapore, 2019

[7]. Biswal, Sudhansu Mohan, Sanjit Kumar Swain, Biswajit Baral, Debasish Nayak, Umakanta Nanda, **Satish Kumar Das** & Dhananja Tripthy. "Performance Analysis of Staggered Heterojunction based SRGTFET biosensor for health IoT application. "In 2019 Devices for Integrated Circuit (DevIC), pp.493-496. IEEE, 2019.

[8]. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, Sudhansu Mohan Biswal, Dhananjaya Tripthy, Sanjit Kumar Swain, Biswajit Baral and **Satish Kumar Das.** "A Novel Driverless SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination. "In 2019 Devices for Integrated Circuit (DevIC), pp.314-317. IEEE, 2019.

[9]. Tripathy, Dhananjaya, Debasish Nayak, Sudhansu Mohan Biswal, Sanjit Kumar Swain, Biswajit Baral, and **Satish Kumar Das.** "A Low Power LNA using Current Reused Technique for UWB Application. "In 2019 Devices for Integrated Circuit (DevIC), pp.310-313. IEEE, 2019.

[10]. Baral, Biswajit, Sudhansu Mohan Biswal, Sanjit Swain, **Satish Kumar Das,** Debasish Nayak and Dhananjaya Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC pplications. "In 2019 Devices for Integrated Circuit (DevIC), pp.505-509. IEEE, 2019.

[11]. **Das, Satish K.,** Sanjit K. Swain, Sudhansu M. Biswal**,** Debasish Nayak, Umakanta Nanda, Biswajit Baral and Dhananjaya Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET. "In 2019 Devices for Integrated Circuit (DevIC), pp.365-369. IEEE, 2019.

[12]. **kumar Das, S.,** Biswal, S.M., Baral, B. and Giri, L., 2021, December. Performance Analysis of Heterojunction Tunnel FET Biosensor. In 2021 19th OITS International Conference on Information Technology (OCIT)(pp.433-436). IEEE.

[13]. Singh, K.C., Biswal, S.M., Baral, B., **Das, S.K**. and Khuntia, P., 2022, November. Study on Sensitivity Parameters of Staggered Heterojunction Gate Stack Tunnel FET Biosensor. In 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON) (pp. 632-636). IEEE.

[14]. **Das, S.K**., Biswal, S.M., Swain, S.K. and Baral, B., 2020. Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET. In ICICCT 2019–System Reliability, Quality Control, Safety, Maintenance and Management: Applications to Electrical, Electronics and Computer Science and Engineering (pp. 803-812). Springer Singapore.

ANY OTHER

Book Chapter
Conferences attended

BOOK CHAPTER

[1]. **Das, S.K.**, Biswal, S.M., Swain, S.K. and Baral, B., 2020. Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET. In ICICCT 2019–System Reliability, Quality Control, Safety, Maintenance and Management: Applications to Electrical, Electronics and Computer Science and Engineering (pp. 803-812). Springer Singapore.

SOFTWARE SKILLS

1. Silvaco
2. TCAD
3. MATLAB
4. Labview