



## Sudhansu Kumar Pati, Ph.D.

**Designation** : Addl. Professor  
**Department** : Department of Electronics Engineering  
(JOINED THE INSTITUTE IN YEAR2004)  
**Contact** : 9658907001 (M)  
**Email** : sudhansu@silicon.ac.in

### RESEARCH INTERESTS

- ✓ The research interests are in the field of semiconductor devices through modeling and simulation.
- ✓ Mainly focused on the physics and the characterization of Metal-Oxide-Semiconductor (MOS) field-effect-transistors, High Speed Electron Mobility Transistors (HEMT) and MOS-HEMT Devices.
- ✓ Investigating the new channel material of the MOS device structures to overcome the shortfall of performances in the new trend technology.
- ✓ To explore the new CMOS structures to fit in SOC fabrication by the noise and RF analysis.

### Academic Qualifications

- PhD(ECE), Jadavpur University, Kolkata, West Bengal, India, (13/05/2015)
- M.TECH (EE), Electronic Systems and Communication, NIT, Rourkela, Odisha, India, (June-2004)

### Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience- 20 years
- ✓ Research Experience- 13 years

## PUBLICATIONS

### JOURNALARTICLES & CONFERENCE PAPERS

- [1]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar, "Flicker and thermal noise in an n-channel underlap DG FinFET in a weak inversion region", Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-6, February 2013.
- [2]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar, "Impact of gate length and barrier thickness on performance of InP/InGaAs based Double Gate Metal-Oxide-Semiconductor Heterostructure Field-Effect Transistor (DG MOS-HFET)", Superlattices and Microstructures - ELSEVIER Publishers, Vol. 55, Pages:8-15, 2013.

- [3]. **Sudhansu Kumar Pati**, KalyanKoley, ArkaDutta, N. Mohan Kumar and Chandan Kumar Sarkar," A New Approach to Extract the RF Parameters of Asymmetric DG MOSFET with NQS Effect", Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-5, November 2013.
- [4]. **Sudhansu Kumar Pati**, Kalyan Koley, Arka Dutta, N. Mohan Kumar and Chandan Kumar Sarkar," Study of body and oxide thickness variation on analog and RF performance of underlap DGMOSFETs", Microelectronics Reliability-Elsevier Publishers,Vol. 54, No. 6–7, Pages: 1137–1142, 2014.
- [5]. Hemant Pardeshi, **Sudhansu Kumar Pati**, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar," Effect of underlap and gate length on device performance of an AllnN/GaN underlap MOSFET", Journal of Semiconductors, IOP Science publishers, Vol. 33, No. 12, pp. 1-7, 2012.
- [6]. Hemant Pardeshi, **Sudhansu Kumar Pati**, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar, "Investigation of asymmetric effects due to gate misalignment, gate bias and underlap length in III–V heterostructure underlap DG MOSFET", Physica E: Low-dimensional Systems and Nanostructures, Elsevier, Vol. 46, pp. 61–67, 2012.
- [7]. Hemant Pardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar, "Comparative Assessment of III–V Heterostructure and Silicon Underlap Double Gate MOSFETs", Semiconductors, Springer, Vol. 46, No. 10, pp. 1299– 1303, 2012.
- [8]. Godwin Raj, Hemant Pardeshi, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar," Physics Based Charge and Drain Current Model for AlGaIn/GaN HEMT Devices", Journal of Electron Devices, Vol. 14, pp. 1155-1160, 2012. ISSN: 1682-3427.
- [9]. Godwin Raj, Hemant Pardeshi, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar," Polarization based charge density drain current and small-signal model for nano-scale AllnGaIn/AlIn/GaN HEMT devices", Superlattices & Microstructures, Elsevier, Vol.54, pp.188-203, 2013.
- [10]. Hemant Pardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar," Influence of barrier thickness on AllnN/GaN underlap DG MOSFET device performance", Superlattices and Microstructures, Elsevier, Vol. 60, pp. 47–59, 2013.
- [11]. Hemant Pardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar," Performance assessment of gate material engineered AllnN/GaN underlap DG MOSFET for enhanced carrier transport efficiency", Superlattices and Microstructures, Elsevier, Vol. 60, pp. 10–22, 2013.
- [12]. Sanjit Kumar Swain, Sarosij Adak, **Sudhansu Kumar Pati**, Hemant Pardeshi and Chandan Kumar Sarkar," Analysis of flicker and thermal noise in p-channel Underlap DG FinFET", Microelectronics Reliability, Elsevier, Vol. 54, No. 8, pp. 1549–1554, 2014.
- [13]. Sarosij Adak, Sanjit Kumar Swain, Avtar Singh, Hemant Pardeshi, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar," Study of HfAlO/AlGaIn/GaN MOS-HEMT with source field plate structure for improved breakdown voltage", Physica E: Low-dimensional Systems and Nanostructures, Elsevier, Vol. 64, pp. 152–157, 2014. ISSN: 1386- 9477,
- [14]. Sarosij Adak, Arghyadeep Sarkar, Sanjit Swain, Hemant Pardeshi, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "High Performance AllnN/AlIn/GaN p-GaN Back Barrier Gate-Recessed Enhancement-Mode HEMT", Superlattices & Microstructures, Elsevier, Vol. 75, pp. 347–357, 2014.
- [15]. Sanjit Kumar Swain, Sarosij Adak, Bikash Sharma, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Effect of Channel Thickness and Doping Concentration on Sub-Threshold Performance of Graded Channel and Gate Stack DG MOSFETs", Journal of Low Power Electronics, American Scientific Publishers, Vol. 11, pp. 366-372, 2015.

- [16]. Sanjit Kumar Swain, Arka Dutta, Sarosij Adak, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Influence of channel length and highK oxide thickness on subthreshold analog/RF performance of graded channel and gate stack DG-MOSFETs", *Microelectronics Reliability*, Elsevier, Vol. 61, pp. 24-29, 2016.
- [17]. Sanjit Kumar Swain, Sarosij Adak, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar, "Impact of InGaN back barrier layer on performance of AlInN/AlN/GaN MOS-HEMTs", *Superlattices and Microstructures*, Elsevier, Vol. 97, pp. 258-267, 2016.
- [18]. Sarita Misra, Sudhansu Mohan Biswal, Biswajit Baral, Sanjit Kumar Swain, Angsuman Sarkar, **Sudhansu Kumar Pati**, "Analytical modelling of a Cyl-JLAM MOSFET in the subthreshold region using distinct device geometry", *Journal of Computational Electronics*, Springer, Vol. 20, pp.480-491, 2021/2.
- [19]. Sarita Misra, Sudhansu Mohan Biswal, Biswajit Baral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, "Study of Analog/Rf and Stability Investigation of Surrounded Gate Junctionless Graded Channel MOSFET(SJLGC MOSFET)" *Silicon*, Springer, Vol. 14, pp.6391-6402, 2021.
- [20]. SaritaMisra, Sudhansu Mohan Biswal, Biswajit Baral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, " Study of DC and Analog /RF performances Analysis of Short Channel surrounded Gate junctionless Graded Channel Gate Stack MOSFET" *Transactions on Electrical and Electronic Materials*, Springer, Vol. 24, pp.346-355, 2023.
- [21]. Sarita Misra, Sudhansu Mohan Biswal, Biswajit Baral, **Sudhansu Kumar Pati**, "Investigation of graded channel effect on analog/linearity parameter analysis of junctionles ssurrounded gate graded channel MOSFET" *SN Applied Sciences*, Springer, Vol. 5, article number-384, 2023.
- [22]. **Sudhansu Kumar Pati**, Arghyadeep Sarkar, Hemant Pardeshi, Godwin Raj, N Mohan Kumar and Chandan Kumar Sarkar, "Analytical Drain Current Model for Symmetrical Gate Underlap DGMOSFET", *IJCA Proceedings on International Conference on Communication, Circuits and Systems 2012* iC3S(3):26-28, June 2013.
- [23]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N Mohan kumar and Chandan Kumar Sarkar, "Comparison study of Drain Current, Subthreshold Swing and DIBL of III-V Heterostructure and Silicon Double Gate MOSFET", *IJECT* ,Vol. 4, Issue spl - 1, Jan - March 2013.
- [24]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N Mohan kumar and Chandan Kumar Sarkar, "Performance Comparison of III-V Heterostructure and Silicon Double Gate MOSFET", *2nd International Conference on Advances in Engineering & Technology (ICAET2012)*, March 28 & 29, 2012.
- [25]. SaritaMisra, Sudhanshu Mohan Biswal, Biswajit Baral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, „Study of Effect of downscaling on the Analog/RF Performance of Gate all Around JLMOSFET" , 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 234-241, DOI:10.1109/EDKCON.2018.8770424, Corpus ID: 198929394.
- [26]. Sudhanshu Mohan Biswal, Biswajit Baral, Sanjit Kumar Swain, **Sudhansu Kumar Pati**, "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET" 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 344-348, DOI: 10.1109/EDKCON.2018.8770447.
- [27]. S. Misra, K. P. Swain, S. M. Biswal, **S. K. Pati**, J. K. Das," Analog/RF Performance Analysis of Downscaled Cylindrical Gate Junctionless Graded Channel MOSFET" *Advances in Intelligent Computing and Communication*, conference paper, pp. 101-108, 2022.
- [28]. Pradipta Kumar Jena , Prasanta Kumar Khuntia , Biswajit Baral, **Sudhansu Kumar Pati**, Impact of Gate engineering on Analog, RF Performance of Nanoscale Barriered TM Heterostructure DG-MOSFET" 2022 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 646-649, 2022.

- [29]. Prasanta Kumar Khuntia, Biswajit Baral , Sudhansu Mohan Biswal, **Sudhansu Kumar Pati**, "III-V Heterostucture Transistor with Underlap: A Comparitive Study and Performance Investigation" 2022 IEEE Electron Devices Kolkata Conference (EDKCON), pp. 646-649, 2022.
- [30]. Srikrishna Bardhan, Pradipta Kumar Jena, Sarita Misra, Sanghamitra Das, Biswajit Baral, **Sudhansu Kumar Pati**, "Analytical Volume Inversion Charge density Modeling of SGCG DG MOSFET in the presence of Interfacial Traps", IEEE 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), pp. 1-6, 2023.
- [31]. Pradipta Kumar Jena, Sanghamitra Das, Srikrishna Bardhan, Sarita Misra, Biswajit Baral, **Sudhansu Kumar Pati**," Low Frequency Noise Analysis in AlGaIn/GaN HEMTs", IEEE 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), pp. 1-4, 2023.

## ANY OTHER

---

Book Chapter  
Conferences attended