Sudhansu Mohan Biswal, Ph.D.

Designation : Associate Professor

Department : Department of Electronics & Communication Engineering

(JOINED THE INSTITUTE IN JAN 2007)

Contact : + 91 - 9438788420, 9861863662

Email : sudhansu.mohan@silicon.ac.in

Research Interests

- ✓ Semiconductor devices modeling and simulation study
- ✓ VLSI Design
- ✓ IoT & Automation Control

Academic Qualifications

Ph. D. (Engg) Maulana Abul Kalam Azad University of Technology, West Bengal, India

M.Tech. (Electronics & Communication Engg.), BPUT, Odisha

B. Tech. (AE&I), Utkal University, Odisha

Specialisation : Nano Electronics & Device Engg.

Teaching Experience/Industrial Experience/Research Experience

Teaching Experience : More than 22 years

Research Experience : More than 14 years

PUBLICATIONS

JOURNAL ARTICLES & CONFERENCE PAPERS

PATENTS

Title of the Invention : Smart Management of Food Storage and Waste Reduction using Block Chain Technology

Application No. : **202141026736 A**

Date of filing of Application : **16/06/2021**, Publication Date : **25/06/2021**

The Patent Office Journal No. : **26/2021** Dated **25/06/2021**

JOURNAL

[1]. **Biswal, S.M**., Baral, B., De, D. and Sarkar, A., "Analytical subthreshold modeling of dual material gate engineered nano-scale junctionless surrounding gate MOSFET considering ECPE" ***Superlattices and Microstructures*, published by Elsevier** B.V., vol. *82*, pp.103-112., 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140

[2]. **Biswal, S.M**., Baral, B., De, D. and Sarkar, A., "Study of effect of gate-length downscaling on the analog/RF performance and linearity investigation of InAs-based nanowire Tunnel FET" ***Superlattices and Microstructures***, **published by Elsevier** vol. 91, pp. 319-330, 2016 (**SCI Indexed**) **Impact Factor: 2.123**, 5-Year Impact Factor: 2.140

[3]. **Biswal, S. M**., Baral, B., *D.* De, and Sarkar A. "Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET" *Advances in Industrial Engineering and Management*, published by **American Scientific Publishers, USA,** vol. 5, no. 1, pp. 150-156, 2016, DOI: 10.7508/aiem. 2016.01.005.

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[8]. Swain, S., **Biswal, S. M***.,* *Das* S., Adak S., Baral B. "Performance Comparasion of InAs based DG-MOSFET with respect to SIO2 and Gate stack configuration"**Journal of Nanoscience & Nanotechnology-Asia,published by Betham Science.**Vol.9, 2019 **(SCI Indexed) Impact factor : 0.78**

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[11]. Das, S.K., Nanda, U., **Biswal, S.M**., Pandey, C.K. and Giri, L.I., 2021. Performance Analysis of Gate-Stack Dual-Material DG MOSFET Using Work- Function Modulation Technique for Lower Technology Nodes. **Silicon**,**Springer** pp.1-9.

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[2]. Biswajit Baral, **Sudhansu M Biswal**, et al. "Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th &15th October 2014

[3]. **Sudhansu Mohan Biswal**, Biswajit Baral, et al. "Simulation and comparative study on Analog/RF performance of Silicon and InAs nanowire Tunnel FET " TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016), (MAKAUT).

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[15]. B.Baral, P.priya, R.Nayak, S. Pradhan, **S.M.Biswal** "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM- Heterostructure DG-MOSFET" IEEE International Conference on Communication and Electronics System (ICCES-2017), 19th-20th October, 2017, Coimbatore

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ANY OTHER

Book Chapter
Conferences attended

BOOK CHAPTER

[1]. **Sudhansu Mohan Biswal**, Sanjit Kumar Swain, Jyoti Ranjan Sahoo, Anupam K. Swain, Kunal Routaray, Umakanta Nanda, Birendra Biswal, "A Comparative Study Of Junctionless Triple-Material Cylindrical Surrounding Gate Tunnel Fet", Springer Book series on Microelectronics, Electromagnetics & Telecommunications pp 793-801, 03 November 2018.

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[3]. Sanjit Kumar Swain, **Sudhansu Mohan Biswal**, Umakanta Nanda, D. Siva Patro, Suraj Kumar Nayak, Birendra Biswal, "Impact of P-Gan Gate Length On Performance Of Algan/Gan Normally-Off Hemt Devices", Springer Book series on Microelectronics, Electromagnetics and Telecommunications pp 803-809, 03 November 2018.

[4]. Das, Sanghamitra, Taraprasanna Dash, Biswajit Baral, **Sudhansu Mohan Biswal,** Devika Jena, and Eleena Mohapatra. "Analytical modeling of nanoscale advance devices and their reliability aspects." In Nanoelectronics: Physics, Materials and Devices, pp. 385-408. Elsevier, 2023. DOI : https://doi.org/10.1016/C2020-0-03814-4

SOFTWARE SKILLS

1. Silvaco
2. TCAD
3. MATLAB
4. Labview
5. Pspise
6. PLC/SCADA