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Department : Département of Electronics & Communication Engineering.
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RESEARCH INTERESTS

- Semiconductor Devices Modeling and Simulation study
- VLSI Design

Academic Qualifications

- Ph. D. (Electronics& Communication) in MAKAUT, West Bengal, India
- M. Tech. (Electronics & Communication Engg.), BPUT, Odisha
- B. Tech. (ETC), BPUT, Odish

Teaching Experience/Industrial Experience/Research Experience

- Teaching Experience : More than 21 years
- Research Experience : More than 17 years

PUBLICATIONS

PATENTS :

Title of the Invention : Smart Management of Food Storage and Waste Reduction using Block Chain Technology

Application No. : **202141026736 A**

Date of filing of Application : **16/06/2021**, Publication Date : **25/06/2021**

The Patent Office Journal No. : **26/2021** Dated **25/06/2021**

JOURNALS:

- J1. **Baral, B.**, Das, A. K., De, D., and Sarkar, A. "An analytical model of triple-material double-gate metal oxide-semiconductor field-effect transistor to suppress short-channel effects" *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, published by John Wiley & Sons Inc., vol. 29, no. 1, pp. 47-62, 2015, doi:10.1002/jnm.2044. doi.org/10.1002/jnm.2044 (**SCI Indexed**)

- J2. **Baral, B.**, Biswal, S, De, D, and Sarkar, A. "Effect of gate-length downscaling on the analog/RF and linearity performance of InAs-based nanowire tunnel FET" *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, published by John Wiley & Sons Inc., vol. 30, no. 3-4, 2016, doi: 10.1002/jnm.2186, **(SCI Indexed)**
- J3. **Baral, B.**, Biswal, S. M., De, D., and Sarkar A. " RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET" *Simulation: Transactions of the Society for Modeling and Simulation International*" published by SAGE Publications, United Kingdom, vol. 1-9, 2017 **(SCI Indexed)**, doi.org/10.1177/00375497177043
- J4. **Baral, B.**, Biswal, S. M., De, D., and Sarkar A. "Effect of gate length downscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications & it's comparative study with conventional Mosfet" *Advances in Industrial Engineering and Management*, published by American Scientific Publishers, USA vol. 5, no. 1, 2016, pp. 130-137, DOI: 10.7508/aiem.2016.01.005.
- J5. Biswal, S.M., **Baral, B.**, De, D. and Sarkar, A., "Analytical subthreshold modeling of dual material gate engineered nano-scale junctionless surrounding gate MOSFET considering ECPE" *Superlattices and Microstructures*, published by Elsevier B.V., vol. 82, pp.103-112., 2016 **(SCI Indexed)** Impact Factor: 2.123, doi.org/10.1016/j.spmi.2015.02.018
- J6. Biswal, S.M., **Baral, B.**, De, D. and Sarkar, A., "Study of effect of gate-length downscaling on the analog/RF performance and linearity investigation of InAs-based nanowire Tunnel FET" *Superlattices and Microstructures*, vol. 91, pp. 319-330, 2016 **(SCI Indexed)** Impact Factor: 2.123, doi.org/10.1016/j.spmi.2016.01.021
- J7. Biswal, S. M., **Baral, B.**, D. De, and Sarkar A. "Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET" *Advances in Industrial Engineering and Management*, published by American Scientific Publishers, USA, vol. 5, no. 1, pp. 150-156, 2016, DOI: 10.7508/aiem.2016.01.005.
- J8. Biswal, Sudhansu Mohan, **Biswajit Baral**, Debashis De, and A. Sarkar. "Simulation and comparative study on analog/RF and linearity performance of III-V semiconductor-based staggered heterojunction and InAs nanowire (nw) Tunnel FET." *Microsystem Technologies* (2017): 1-7. doi.org/10.1007/s00542-017-3642-z
- J9. Sanjit Kumar Swain*, Sudhansu Mohan Biswal, Satish Kumar Das, Sarasij Adak and **Biswajit Baral**, "Performance Comparison of InAs Based DG-MOSFET with Respect to SiO₂ and Gate Stack Configuration", *Nanoscience & Nanotechnology-Asia*(2019) <https://doi.org/10.2174/2210681209666190919094434>
- J10. Misra, S., Biswal, S.M., **Baral, B.**, Swain, S.K., Sarkar, A. and Pati, S.K., 2020. Analytical modelling of a Cyl-JLAM MOSFET in the subthreshold region using distinct device geometry. *Journal of Computational Electronics*, pp.1-12. doi.org/10.1007/s10825-020-01560-z
- J11. Misra, S., Biswal, S.M., **Baral, B.**, Swain, S.K. and Pati, S.K., 2021. Study of Analog/Rf and Stability Investigation of Surrounded Gate Junctionless Graded Channel MOSFET (SJLGC MOSFET). *Silicon*, pp.1-12. doi.org/10.1007/s12633-021-01397-6
- J12. Misra, S., Biswal, S.M., **Baral, B.** et al. Study of DC and Analog/RF Performances Analysis of Short Channel Surrounded Gate Junctionless Graded Channel Gate Stack MOSFET. *Trans. Electr. Electron. Mater.* (2023). doi.org/10.1007/s42341-023-00455-7
- J13. Jena, D., Das, S., **Baral, B.**, Mohapatra, E. and Dash, T., 2023. Linearity improvement in graded channel AlGaIn/GaN HEMTs for high-speed applications. *Physica Scripta*, 98(10), p.105936,doi10.1088/1402-4896/acf3b6

CONFERENCES:

- C1. **Biswajit Baral**, Sudhansu Mohan Biswal, et al. " Performance Investigation of III-V Heterosturucture Underlap Double Gate MOSFET for System-On-Chip Application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).
- C2. **Biswajit Baral**, Sudhansu Mohan Biswal, et al. "Performance Analysis of Downscaled Triple Material Double Gate Junctionless MOSFET using High-K for Analog/mixed signal System-on-chip Applications." TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016). (MAKAUT)
- C3. **Biswajit Baral**, Jagruti Padhee, et al. "Effect of gate length downscaling on RF/Analog and Linearity performance of a Junctionless Double Gate MOSFET for Analog/mixed signal System-on-chip applications & it's comparative study with conventional MOSFET" 1st International conference on Devices for Integrated Circuits (DevIC-2016).
- C4. **Biswajit Baral**, Sudhansu M Biswal, et al. " Effect of gate length downscaling on RF and Analog performance of a Junctionless Double Gate Mosfet for Analog/mixed signal System-on-chip applications." International conference Nanocon 014, Pune, 14th & 15th October 2014.
- C5. Sudhansu M Biswal, **Biswajit Baral**, et al. " Study of effect of gate-length downscaling on the Analog/RF performance of Tunnel FET." International conference Nanocon 014, Pune, 14-15th October 2014.
- C6. Sudhansu Mohan Biswal, **Biswajit Baral** , et al. " Simulation and comparative study on Analog/rF performance of Silicon and InAs nanowire Tunnel FET " TEQIP-II sponsored 1st International Conference on Nanocomputing & Nanobiotechnology (NanoBioCon-2016), (MAKAUT).
- C7. Sudhansu Mohan Biswal, **Biswajit Baral**, et al. " Analog/RFand Linearity Performance of staggered heterojunction Nanowire Tunnel FET for low power application." 2nd International conference on Devices for Integrated Circuits (DevIC-2017).
- C8. Sudhansu Mohan Biswal, **Biswajit Baral**, et al. " Analog/RF performance and linearity investigation of Si-based double gate Tunnel FET" 1st International conference on Devices for Integrated Circuits (DevIC-2016).
- C9. Prateek Singh, Sahed Akhtar, **Biswajit Baral**, " A Comparision study of RF and Analog Performance of a JL-DG MOSFET with different types of Channel material through simulation" 1st International conference ICIT-2014,23rd-24th Dec 2014, SIT Bhubaneswar.
- C10. Payel Chand, Nikhil Agarwal, **Biswajit Baral**, " Comparative Study of Gate Underlap and Overlap in Junction-less DG-MOSFET with High k-Spacer through simulation" National conference on Recent Advances on electrical & electronics engg. (NCRAEEE-15),27th-28th March, 2015, GIFT, Bhubaneswar.
- C11. R.Pattnaik,**B.Baral** et all. " Comparative performance analysis of JL DG-MOSFET with Underlap JL DG-MOSFET " National conference on Recent Advances on electrical and electronics engg. (NCRAEEE-15), 27th -28th March,2015,GIFT,Bhubaneswar
- C12. R.K.Majhi, S.Das, S.K.Kar, **B.Baral**" RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications " 1st International conference ICIT-2014,23rd -24th Dec 2014,SIT Bhubaneswar.
- C13. **B.Baral**, P.priya, R.Nayak, S. Pradhan,S.M.Biswal "Impact of Gate engineering on Analog, RF & Linearity Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET"IEEE International Conference on Communication and Electronics System(ICCES-2017),19th-20th October 2017, Coimbatore

- C14. Sanjit Swain, Sarosij Adak, Sudhansu Mohan Biswal, **Biswajit Baral**, and Saradiya Parija. "Comparison of Linearity Performance of InAs Based DG-MOSFETs with Gate Stack, SiO₂ and HfO₂." In *2018 IEEE Electron Devices Kolkata Conference (EDKCON)*, pp. 242-246. IEEE, 2018.
- C15. Das, Satish Kumar, Sudhansu Mohan Biswal, Sanjit Kumar Swain, and **Biswajit Baral**. "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET." In *International Conference on Intelligent Computing and Communication Technologies*, pp. 803-812. Springer, Singapore, 2019.
- C16. Biswal, Sudhansu Mohan, **Biswajit Baral**, Sanjit Kumar Swain, and Sudhansu Kumar Pati. "Performance Analysis of Down Scaling Effect of Si based SRG Tunnel FET." In *2018 IEEE Electron Devices Kolkata Conference (EDKCON)*, pp. 344-348. IEEE, 2018.
- C17. Biswal, Sudhansu Mohan, Sanjit Kumar Swain, **Biswajit Baral**, Debasish Nayak, Umakanta Nanda, Satish Kumar Das, and Dhananjan Tripathy. "Performance Analysis of Staggered Heterojunction based SRG TFET biosensor for health IoT application." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 493-496. IEEE, 2019.
- C18. Nayak, Debasish, Umakanta Nanda, Prakash Kumar Rout, Sudhansu Mohan Biswal, Sanjit Kumar Swain, **Biswajit Baral**, and Satish Kumar Das. "A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 314-317. IEEE, 2019. DOI: 10.1109 /DEVIC.2019.8783644
- C19. Tripathy, Dhananjan, Debasish Nayak, Sudhansu Mohan Biswal, Sanjit Kumar Swain, **Biswajit Baral**, and Satish Kumar Das. "A Low Power LNA using Current Reused Technique for UWB Application." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 310-313. IEEE, 2019.
- C20. **Baral, Biswajit**, Sudhansu Mohan Biswal, Sanjit Swain, Satish Kumar Das, Debasish Nayak, and Dhananjan Tripathy. "RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 505-509. IEEE, 2019.
- C21. Das, Satish K., Sanjit K. Swain, Sudhansu M. Biswal, Debasish Nayak, Umakanta Nanda, **Biswajit Baral**, and Dhananjan Tripathy. "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET." In *2019 Devices for Integrated Circuit (DevIC)*, pp. 365-369. IEEE, 2019. DOI: 10.1109/DEVIC.2019.8783740
- C22. Kumar Das Satish, Sudhansu Mohan Biswal, **Biswajit Baral**, and Lalatindu Giri. "Performance Analysis of Heterojunction Tunnel FET Biosensor." In *2021 19th OITS International Conference on Information Technology (OCIT)*, pp. 433-436, doi: 10.1109/OCIT53463.2021.00090, IEEE, 2021.
- C23. Das, S.K., Biswal, S.M., Swain, S.K. and **Baral, B.**, 2020. Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET. In *ICICCT 2019–System Reliability, Quality Control, Safety, Maintenance and Management: Applications to Electrical, Electronics and Computer Science and Engineering* (pp.803-812). Springer Singapore.
- C24. Singh, K.C., Biswal, S.M., **Baral, B.**, Das, S.K. and Khuntia, P., 2022, November. Study on Sensitivity Parameters of Staggered Heterojunction Gate Stack Tunnel FET Biosensor. In *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 632-636). IEEE.
- C25. Jena, P.K., Khuntia, P., **Baral, B.** and Pati, S.K., 2022, November. Impact of Gate engineering on Analog, RF Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET. In *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 646-649). IEEE.
- C26. Khuntia, P., **Baral, B.**, Biswal, S.M. and Pati, S.K., 2022, November. III-V Heterostructure Transistor with Underlap: A Comparative Study and Performance Investigation. In *2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 338-343). IEEE.

- C27. P. K. Khuntia, K. C. Singh, **B. Baral** and S. M. Biswal, "Performance Analysis of Triple Material Double Gate MOSFET for Biosensing Application," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 1-5, doi: 10.1109/CCPIS59145.2023.10291323.
- C28. K. C. Singh, P. K. Khuntia, P. Mohanty, S. M. Biswal, **B. Baral** and S. K. Swain, "Comparative Study of InAs Based Tunnel FET(TFET) Biosensor," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 01-04, doi: 10.1109/CCPIS59145.2023.10291959.
- C29. S. Bardhan, P. K. Jena, S. Misra, S. Das, **B. Baral** and S. K. Pati, "Analytical Volume Inversion Charge density Modeling of SGCG DG MOSFET in the presence of Interfacial Traps," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp. 1-6, doi: 10.1109/CCPIS59145.2023.10291376.
- C30. R. K. Pattanaik, **B. Baral** and M. N. Mohanty, "A Machine Learning Approach for Voice Modelling and Identification," *2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS)*, Bhubaneswar, India, 2023, pp.1-5, doi: 10.1109/CCPIS59145.2023.10291252

BOOK CHAPTER

1. Das, Sanghamitra, Taraprasanna Dash, **Biswajit Baral**, Sudhansu Mohan Biswal, Devika Jena, and Eleena Mohapatra. "Analytical modeling of nanoscale advance devices and their reliability aspects." In *Nanoelectronics: Physics, Materials and Devices*, pp. 385-408. Elsevier, 2023. DOI : <https://doi.org/10.1016/C2020-0-03814-4>