Joy Chowdhury, Ph.D.(submitted), M.Tech

Designation: Asst. Professor

Department: Department of Electronics and Communication Engineering (JOINED THE INSTITUTE IN SEPTEMBER, 2024)

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RESEARCH INTERESTS

Advanced CMOS device-circuit co-design, FET biosensors, analytical modelling of nanodevices, ASIC Design, Reconfigurable System Design, Low Power architectures, hardware security, in-circuit computation, IoT based VLSI designs, AI in VLSI

Academic Qualifications

Ph. D.	:	NIT Rourkela, Rourkela, Odisha
M. Tech.	:	KIIT University, Bhubaneswar, Odisha
Specialization	:	VLSI Design and Embedded Systems

Teaching Experience/Industrial Experience/Research Experience

Teaching Experience	: 3.5 Years
Project Experience	: 6 months (SMDP C2S,MeitY,Govt. of India)
Research Experience	: 6 Years

PUBLICATIONS

JOURNAL ARTICLES & CONFERENCE PAPERS

JOURNALS:

[1] J. Chowdhury, K. Mahapatra, A. Sarkar and J. K. Das, "An Analytical Model Accounting for the Pertinence of Hybrid Tunneling in Bio-TFETs," in IEEE Transactions on Nanotechnology, vol. 23, pp. 658-664, 2024, doi: 10.1109/TNANO.2024.3462605 (SCI, IF-2.967)

[2] Joy Chowdhury[1,2,*], Kamalakanta Mahapatra[2], Angsuman Sarkar[3], J K Das[4] and Alexander Kloes, "Design and performance investigation of tunnel-FET based energy efficient approximate and accurate adders targeted towards low power IoT nodes" in *Physica Scripta, IOP Publishing*, vol. 99, no. 11, 2024, **doi:** 10.1088/1402-4896/ad881d (SCI, IF-2.9)

[3] Joy Chowdhury, Angsuman Sarkar, Kamalakanta Mahapatra, Jitendra Kumar Das," More-than-Moore Steep Slope Devices for Higher Frequency

Switching Applications: A Designer's Perspective," Physica Scripta, Volume 99, Number 4, March 2024, DOI: 10.1088/1402-4896/ad2da2 (SCI, IF-2.9)

[4] Joy Chowdhury, Angsuman Sarkar, Kamalakanta Mahapatra, Jitendra Kumar Das, "Analytical modeling of dielectrically modulated broken-gate tunnel FET biosensor considering partial hybridization effect," Computers and Electrical Engineering, Volume 99, 2022, https://doi.org/10.1016/j.compeleceng.2022.107859 (SCI, IF- 4.3)

[5] Chowdhury, J., Sarkar, A., Mahapatra, K. and Das, J.K. , "Novel center potential based analytical sub-threshold model for dual metal broken gate TFET", Circuit World, Vol. 50 No. 1, pp. 1-8., 2020, https://doi.org/10.1108/CW-06-2020-0117 (SCIE, IF-0.9)

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[1] J. Chowdhury, A. Sarkar, J. K. Das and K. Mahapatra, "Tunnel FET based Standard Logic Cell Implementation: A Circuit Perspective," 2023 2nd Edition of IEEE Delhi Section Flagship Conference (DELCON), Rajpura, India, 2023, pp. 1-5, doi: 10.1109/DELCON57910.2023.10127359

[2] J. Chowdhury, A. Sarkar, K. Mahapatra and J. K. Das, "Analytical Drain Current Model for Super-Threshold Region of Double Gate Tunnel FET," 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), Kolkata, India, 2020, pp. 1-4, doi: 10.1109/VLSIDCS47293.2020.9179867

[3] J. Chowdhury, A. D. Deyasi, A. Sarkar and K. Mahapatra, "Novel Threshold Voltage Model Incorporating Band-to-Band Tunneling in Heterostructure p-MOSFET," 2019 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Rourkela, India, 2019, pp. 373-376, doi: 10.1109/iSES47678.2019.00092.

.[4] R. Roy, J. Chowdhury and J. K. Das, "Analytical study of double gate MOSFET: A design and performance perspective," 2018 2nd International Conference on Inventive Systems and Control (ICISC), Coimbatore, India, 2018, pp. 625-634, doi: 10.1109/ICISC.2018.8398875

[5] Joy Chowdhury, J. K. Das, N. K. Rout, "Implementation of 24T Memristor Based Adder Architecture with improved performance",International Journal of Electrical, Electronics and Data Communication, ISSN: 2320-2084 Volume-3, Issue-6, June-2015, pp- 91-94

[6] Joy Chowdhury, J. K. Das, N.K. Rout "Trignometric Window Function for memristive De- vice Modeling.", 2015 5th International Conference on Advanced Computing & Communi- cation Technologies, PP-157-161, IEEE CPS, DOI- 10.1109/ACCT.2015.25

[7] Joy Chowdhury, J. K. Das, N.K,Rout ,"Implementing Trigonometric Nonlinearity in Linear Ion-drift Memristor Model", IEEE International Conference on Industrial Instrumentation and Control, College of Engineering Pune, pp- 1150-1153, DOI- 10.11.09/IIC.2015.7150921, IEEE CPS

[8] Mohita; Tannu Newar; Tista Roy; Joy Chowdhury; J. K. Das," Design and stability analysis of CNTFET based SRAM Cell" , 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS), pp-1-5,DOI: 10.1109/SCEECS.2016.7509327Engineering & Nano-Technology (IEMENTech 2018), 4-5 May, 2018, pp. 1-4, Kolkata, India.

ANY OTHER

BOOK CHAPTERS

[1] J. K.Das, P.K.Patra, Joy Chowdhury, ADC and DAC for biomedical application in ADC and DAC for biomedical application, Academic Press, Science Direct, 2021, pp. 197-228, https://doi.org/10.1016/B978-0-323-85172-5.00019-8

[2] Joy Chowdhury, Jitendra Kumar Das, Angsuman Sarkar, Kamalakanta Mahapatra, TCAD simulation of emerging nanoscale devices, in Nanoelectronics: Physics, Materials and Devices, Elsevier, 2023, pp. 409-455, https://doi.org/10.1016/B978-0-323-91832-9.00009-9

Invited Lecture and Tutorials

1. Tutorial Chair and Resource Person at EDKCON 2024, Fairfield by Marriot, Kolkata, West Bengal, India
   Tutorial Talk and Hands-on Session: FPGA-in-loop and Hardware-Software Co-simulation. (https://attend.ieee.org/edkcon-2024/sample-page/)

2. Tutorial Chair and Resource Person at IEEE EDS and DevIC 2025, Kalyani Govt. Engineering College, Kalyani, West Bengal, India
   Tutorial Talk and Hand-on Demo : ASIC Design Flow using open source tools : RTL to GDSII (https://attend.ieee.org/devic-2025/committees/)
3. Invited Lecture on Recent Advances in VLSI Design at Pailan Institute of Technology, Kolkata, on November 16-17,2023