Sudhansu Kumar Pati, Ph.D.

Designation : **Addl. Professor**

Department : Department of Electronics & Communication Engg.

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RESEARCH INTERESTS

- ✓ The research interests are in the field of semiconductor devices through modeling and simulation.
- ✓ Mainly focused on the physics and the characterization of Metal-Oxide-Semiconductor (MOS) field-effect-transistors, High Speed Electron Mobility Transistors (HEMT) and MOS-HEMT Devices.
- ✓ Investigating the new channel material of the MOS device structures to overcome the shortfall of performances in the new trend technology.
- ✓ To explore the new CMOS structures to fit in SOC fabrication by the noise and RF analysis.

Academic Qualifications

PhD(ECE), Jadavpur University, Kolkata, West Bengal, India, (13/05/2015)

- M.TECH (EE), Electronic Systems and Communication, NIT, Rourkela, Odisha, India, (June-2004)

Teaching Experience/Industrial Experience/Research Experience

- ✓ Teaching Experience- 20 years
- ✓ Research Experience- 13 years

PUBLICATIONS

JOURNALARTICLES & CONFERENCE PAPERS

[1]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar, “Flicker and thermal noise in an n-channel underlap DG FinFET in a weak inversion region”, Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-6, February 2013.

[2]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar, “Impact of gate length and barrier thickness on performance of InP/InGaAs based Double Gate Metal–Oxide-Semiconductor Heterostructure Field-Effect Transistor (DG MOS-HFET)”, Superlattices and Microstructures - ELSEVIER Publishers, Vol. 55, Pages:8–15, 2013.

[3]. **Sudhansu Kumar Pati**, KalyanKoley, ArkaDutta, N. Mohan Kumar and Chandan Kumar Sarkar," A New Approach to Extract the RF Parameters of Asymmetric DG MOSFET with NQS Effect", Journal of Semiconductors- IOP Publishers, Vol. 34, No. 2, pp. 1-5, November 2013.

[4]. **Sudhansu Kumar Pati**, Kalyan Koley, Arka Dutta, N. Mohan Kumar and Chandan Kumar Sarkar," Study of body and oxide thickness variation on analog and RF performance of underlap DGMOSFETs", Microelectronics Reliability-Elsevier Publishers,Vol. 54, No. 6–7, Pages: 1137–1142, 2014.

[5]. Hemant Pardeshi, **Sudhansu Kumar Pati**, Godwin Raj, N. Mohan Kumar and Chandan Kumar Sarkar," Effect of underlap and gate length on device performance of an AlInN/GaN underlap MOSFET", Journal of Semiconductors, IOP Science publishers, Vol. 33, No. 12, pp. 1-7, 2012.

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[11]. Hemant Pardeshi, Godwin Raj, **Sudhansu Kumar Pati**, N. Mohan Kumar and Chandan Kumar Sarkar," Performance assessment of gate material engineered AlInN/GaN underlap DG MOSFET for enhanced carrier transport efficiency", Superlattices and Microstructures, Elsevier, Vol. 60, pp. 10–22, 2013.

[12]. Sanjit Kumar Swain, Sarosij Adak, **Sudhansu Kumar Pati**, Hemant Pardeshi and Chandan Kumar Sarkar," Analysis of flicker and thermal noise in p-channel Underlap DG FinFET", Microelectronics Reliability, Elsevier, Vol. 54, No. 8, pp. 1549–1554, 2014.

[13]. Sarosij Adak, Sanjit Kumar Swain, Avtar Singh, Hemant Pardeshi, **Sudhansu Kumar Pati** and Chandan Kumar Sarkar," Study of HfAlO/AlGaN/GaN MOS-HEMT with source field plate structure for improved breakdown voltage", Physica E: Low-dimensional Systems and Nanostructures, Elsevier, Vol. 64, pp. 152–157, 2014. ISSN: 1386- 9477,

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[23]. **Sudhansu Kumar Pati**, Hemant Pardeshi, Godwin Raj, N Mohan kumar and Chandan Kumar Sarkar, “Comparison study of Drain Current, Subthreshold Swing and DIBL of III-V Heterostructure and Silicon Double Gate MOSFET”, IJECT ,Vol. 4, Issue spl - 1, Jan - March 2013.

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ANY OTHER

Book Chapter

Conferences attended