Dhananjaya Tripathy, M.Tech.

Designation : Asst. Professor

Department : Department of Electronics & Communication Engg.

(JOINED THE INSTITUTE IN 2014)

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RESEARCH INTERESTS

- ✓ VLSI Design
- ✓ Semiconductor Device

Or As Paragraph

Academic Qualifications

M. Tech In VLSI Signal Processing, VSSUT, Odisha.

B.Tech in Applied Electronics & Instrumentation Engg, CVRCE, Odisha.

Teaching Experience/ Industrial Experience/ Research Experience

- ✓ Teaching&Researchexperience - 12years

PUBLICATIONS

JOURNALARTICLES & CONFERENCE PAPERS

JOURNALS:

[1]. D. Nayak, P. K. Rout, S. S, D. P. Acharya, U. Nanda and **D. Tripathy**, " A novel indirect read technique based SRAM with ability to charge recycle and differential read for low power consumption, high stability and performance", in Proc. of **Microelectronics** Journal (2020).

[2]. **D. Tripthy**, D. P. Acharya, P. K. Rout, S. M. Biswal," Influence of oxide thickness variation on analog and RF performances of SOI FinFET", **FUEE** Journal.

CONFERENCES:

[1]. **D.Tripathy**, S.S.Rout, K.Sethi, "A low power noise cancelling LNA for UWB receiver frontend", in Proc. Of **IEEE** Power, Communication and Information Technolgy Conference (PCITC), pp.442-446, Sept. 2015, Odisha, India

[2]. S.S.Rout, **D.Tripathy**,K.Sethi, "An improved bulk injection cascode mixer for receiver frontend " in National Conferenceon Device and circuits (IEEE), pp. 37-41, Feb. 2016, Odisha ,India

[3]. **D. Tripathy**, T. Manasneha, V. Das, " A single ended TG based 8T SRAM with increased stability and lessdelay", in Proc. Of **IEEE** Recent Trends in Electronics, Information and Communication Technology (RTEICT), pp.1282-1285, May-2017, Bangaluru , India

[4]. **D.Tripathy**, P.Bhadra, " A High Speed Two Stage Operational Amplifier with High CMRR", in Proc. Of **IEEE** Recent Trends in Electronics, Information and Communication Technology (RTEICT), May-2018, Bangaluru, India

[5]. **D.Tripathy**, D. Nayak, S. M. Biswal , S.K. Swain, B.Baral and S.K.Das" A Low Power LNA using Current Reused Technique for UWB Application", in Proc. of ***IEEE*** *Devices for Integrated Circuits (DevIC)*, Mar-2019, kolkata, India.

[6]. D. Nayak, U. Nanda, P.K. Rout, **D.Tripathy**, S.M. Biswal, S.K. Swain, B. Baral and S.K. Das," A Novel Driver less SRAM with Indirect Read for Low Energy Consumption and Read Noise Elimination", in Proc. of ***IEEE*** *Devices for Integrated Circuits(DevIC)*, Mar-2019, kolkata,India.

[7]. B. Baral, S.M. Biswal, S.K. Swain, D. Nayak, S.K. Das,and**D.Tripathy,** " RF/Analog & Linearity performance analysis of a downscaled JL DG MOSFET on GaAs substrate for Analog/mixed signal SOC applications", in Proc. of ***IEEE*** *Devices for Integrated Circuits (DevIC)*, Mar-2019, kolkata,India.

[8]. S. K. Swain, S. K. Das, S.M. Biswal, S. Adak, U. Nanda, A. A. Sahoo, D. Nayak, B. Baral and **D.Tripathy,** " Effect of High-K Spacer on the Performance of Non-Uniformly doped DG-MOSFET", in Proc. of***IEEE****Devices for Integrated Circuits(DevIC)*, Mar-2019, kolkata,India.

[9]. S.K. Das, S. K. Swain, S.M. Biswal, D. Nayak, U. Nanda, B. Baral and **D.Tripathy,** "Effect of High-K Spacer on the Performance of Gate-Stack Uniformly doped DG-MOSFET", in Proc. of ***IEEE*** *Devices for Integrated Circuits (DevIC)*, Mar-2019, kolkata, India.

[10]. S.M. Biswal, S.K. Swain, B. Baral, D. Nayak, U. Nanda, S.K. Das and **D.Tripathy,** "Performance Analysis of Staggeredheterojunctionbased SRG TFET biosensor for health IoT application", in Proc. of ***IEEE*** *Devices for Integrated Circuits(DevIC)*, Mar-2019, kolkata,India.

[11]. S. Sarangi, **D. Tripathy**, S.S. Mahapatra, and S.Rout" A Power and Area Efficient CMOS Bandgap Reference Circuiwith an integrated Voltage Reference Branch", in Proc. of ***Springer*** *Modelling, Simulation, Intelligent Computing (MoSICom-2020)*, BITS-Pilani Dubai Campus.

[12]. **D. Tripathy**, P.K. Rout, D. Nayak, S. M. Biswal, N. Singh" The impact of oxide layer width variation on the performance parmeters of FinFET", in Proc. of***IEEE****Devices for Integrated Circuits(DevIC)*, May-2021, kolkata,India.

[13]. **D. Tripathy**, D.P. Acharya, P.K. Rout and D. Nayak " The impact of GATE thickness variation on FinFET performance parmeters", in Proc. of ***IEEE*** *OITS International Conference on Information Technology (OCIT)*, Dec-2021, Odisha, India.

[14]. N. Singh, S. Dehuri, **D. Tripathy** and A. B. Sahoo, " Real Time Heart Beat Monitoring with LABVIEW", in Proc. of **IEEE** OITS International Conference on Information Technology (OCIT), Dec-2021, Odisha, India, 10.1109/OCIT53463.2021.00014.

[15]. A. K. Tiwary, P.K. Rout, **D. Tripathy** and D. Nayak, " ECG Heartbeat Signal Classification and Detection of CardiacAbnormalitiesusing Deep Learning", in Proc. of **IEEE** Conference on Circuits, Power and Intelligent Systems (CCPIS), Sep-2023, Odisha, India, 10.1109/CCPIS59145.2023.10291586.

[16]. D. P. Pradhan, **D. Tripathy**, S. K. Mohanta and S. M. Biswal, " Intelligent Plant Monitoring System", in Proc. of **IEEE** Conference on Circuits, Power and Intelligent Systems (CCPIS), Sep-2023, Odisha, India, 10.1109/CCPIS59145.2023.10291268.

ANY OTHER

BOOK CHAPTER

BOOK CHAPTER:

Silicon University

PROJECTS:

CONFERENCES ATTENDED